SFP-DD MIS

Management Interface Specification

for

SFP Double Density 2X Pluggable Transceiver

Revision 2.0

September 25, 2020

Abstract: This document defines the SFP-DD Management Interface Specification (MIS) that may be used by 2 lane pluggable modules with host to module management communication based on a Two-Wire-Interface (TWI). This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers.

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Change History:

Revision	Date	Changes
1.0	September 18, 2019	First public release
2.0	September 25, 2020	Following enhancement are made: stage set ready registers added, fault definition now is inline with SFP and limited to laser eye safety or other hazards, IntL/TxFault dual use operation defined, host electrical lanes limited to 2, power classes now consistent with SFP-DD HW definition, updated SFP-DD vs CMIS signals naming.

Foreword

The development work on this specification was done by the SFP-DD MSA, an industry group. The membership of the committee since its formation in May 2017 has included a mix of companies which are leaders across the industry.

Table of Contents

List of Figures

List of Tables

1 Scope and Purpose

This document defines the SFP-DD Management Interface Specification as a generic management interface together with a generic management interaction protocol between hosts and modules. The SFP-DD MIS target audience therefore includes suppliers of modules and transceivers, system manufacturers, and system integrators.

The SFP-DD MIS has been developed to allow host and module software implementers to utilize a common code base across a variety of form factors. It provides a set of core functionality that all modules must implement and a set of optional features whose implementation is advertised in the module memory map. This approach allows host software implementers to read and react to optional module capability advertisements while ensuring interoperability with all modules at a basic level.

Characteristic common to all SFP-DD MIS compliant modules is that management data is transferred over a Two-Wire-Interface (TWI), using a 256 byte addressable memory window, with mechanisms to dynamically page data of a much larger management memory space into the upper half of the host addressable memory window.

The *physical scope* of SFP-DD MIS compliant pluggable modules are 2 lane module form factors. It is a generic management interface based on CMIS 4.0 specification and can be implemented in a variety of both current and future 2 lane form factors. Advertisement fields are provided in the memory map to identify the form factor.

The *functional scope* of SFP-DD MIS compliant modules may range from electrical cable assemblies (hereafter also referred to as modules, unless cable assemblies are specifically mentioned) and active transceiver modules to versatile coherent DWDM modules with integrated framers. A possible classification distinguishes the following functional module types

(1) **data agnostic (basic) system interface modules** such as cable assemblies or active modules that map bit streams from host lanes to media lanes, e.g. SR-2 modules
(2) **data format aware (complex) system interface modules** that perform interface related data processing (such as lane deskewing and FEC codecs), e.g. 100ZR modules
(3) **data link terminals**, i.e. modules with internal framers for media side link termination, comprising framing, mapping, aggregation (multiplexing), switching, or distribution (inverse multiplex) functionality

The *specification scope* of this document release covers data agnostic interface modules with two host electrical lanes and management communication based on a Two-Wire-Interface (TWI) bus as described by NXP UM10204, I2C-bus specification.

2 References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:
CMIS 4.0 (Common Management Interface Specifiation), May 8 2019
Fiber Channel Framing and Signaling FC FS-6
SFP-DD Hardware MSA
OIF CEI 4.0, December 2017
TWI specifications compatible with NXP UM10204, I2C-bus specification and user manual, Rev 6 – 4 April 2014
PTP (Precision Time Protocol): Describes ePPS function.

2.2 Sources

Copies of CMIS may be obtained from www.qsfp-dd.com.

Copies of Common Language Equipment Identification specifications may be obtained from www.commonlanguage.com.

Copies of Fibre Channel FC-FS-6 may be obtained from https://www.incits.org.

Copies of NXP I2C-bus specification may be obtained from https://www.nxp.com/docs/en/user-guide/UM10204.pdf.

Copies of InfiniBand standards may be obtained from the InfiniBand Trade Association (IBTA) (http://www.infinibandta.org).

Copies of IEEE standards may be obtained from the Institute of Electrical and Electronics Engineers (IEEE) (https://www.ieee.org).

Copies of OIF Implementation Agreements may be obtained from the Optical Internetworking Forum (http://www.oiforum.com).

Copies of SFP-DD Hardwear Specifications may be obtained from www.sfp-dd.com.

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS
Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear. The word or term may also be printed in **bold font**.

ORDER OF PRECEDENCE
If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS
Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

Lists sequenced by numbers show an ordering relationship between the listed items.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

NUMBERING CONVENTIONS
The ISO convention of decimal numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

Logical Operations
Logical operators are written in uppercase (OR, AND, NOT) and parentheses are used to clarify precedence.

Numerical Constants
Numerals without suffix are understood as numbers in decimal notation (e.g. 16).
Hexadecimal literals are marked with a suffix 'h' (e.g. 10h), often written with leading zeroes (0010h).
Binary literals are marked with a suffix 'b' (e.g. 10000b), often written with leading zeroes (00010000b).
The suffixes may be omitted for unambiguous cases like 0=0b=0h and 1=1b=1h.
Spaces may be inserted to make long hexadecimal or binary digit strings readable(0001 0000b).

Referencing Module Resources
In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated.

In cases where a status or control aspect is applicable only to lanes after multiplexing or demultiplexing has occurred, the status or control is intended to apply to all lanes in the data path, unless otherwise indicated.
All references to host lanes or media lanes in this document refer to the registers that control or describe those signals. When the term 'lane' is used without reference to 'host' or 'media', a host lane perspective is assumed.

Examples
Examples are printed in grey font for visual differentiation from specification text.

Auxiliary Test
Auxiliary text such as hints or notes are printed in *italic font* for visual differentiation from specification text.

Transition Signals (State Transition Conditions)
State transition conditions in state transition diagrams are also referred to as transition signals (symbolic names ending in S) in analogy to digital state machine circuit specifications.

3 Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May / may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the specification. However, if any feature defined by the specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact when its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word, or field (e.g., a restricted byte uses the same value as defined for a reserved byte).

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

ACK: Acknowledge
ASCII: American Standard Code for Information Interchange (the numerical representation of a character)
BER: Bit Error Rate
CDB: Command Data Block
CDR: Clock and Data Recovery
CLEI: Common Language Equipment Identification
COR: Clear on read
DFB: Distributed Feedback Laser
DWDM: Dense Wavelength Division Multiplexing
EML: Externally Modulated Laser
EPL: Extended Payload Length
ePPS: Enhanced Pulse Per Second
FEC: Forward Error Correction
FERC: Frame Error Count
FP: Fabry-Perot Laser

LPL: Local Payload Length
MBR: Module Boot Record
NACK: Not Acknowledge
OUI: Organizationally Unique Identifier (A unique vendor code assigned by the IEEE)
RO: Read-Only
RW: Readable and Writeable
SDA: bidirectional Serial Data
SCL: unidirectional Serial Clock
TEC: Thermoelectric Cooler
TWI: Two Wire Interface
VCSEL: Vertical Cavity Surface Emitting Laser
VDM: Versatile Diagnostics Monitoring
WDM: Wavelength Division Multiplexing
WR: Writeable

3.3 Definitions

Application: Where used as a defined term, Application is defined as a specific combination of an industry standard host electrical interface and an industry standard module media interface. See Section 6.2 for use.

Bank: A memory map architectural feature that enable set of memory map pages that have the same page numbers, see 7.1.

Checksum: a number derived from a block of digital data for the purpose of detecting errors.

Custom: Custom fields and formats are defined by the module manufacturer and may be unique to a specific vendor.

Data Path: Host electrical and module media lanes grouped together into a logical concept. A data path represents a group of lanes that will be initialized, used and deinitialized together. A data path carries a multi-lane signal.

F16: a SFF-8636 Big Endian 16-bit data type representing an unsigned float value, with 5 bits for base-10 exponent, offset by -24, and 11 bits for mantissa. The format is: $m \cdot 10^{s+o}$ where m ranges from 0 to 2047, s ranges from 0 to 31 and o is fixed at -24. The smallest non-zero number is 1*10^(-24). The largest number supported is 2.047*10^10. Within the 2 bytes of the value (stored lowest byte first), m and s are encoded as follows:

Byte	Bits	Description
1	7:3	Exponent (s)
1	2:0	Mantissa (m), bits 10:8
2	7:0	Mantissa (m), bits 7:0

Flat Memory: Single 256-byte memory implemented without paging

Gray Coding: used with PAM4 modulation. Defines the mapping of 2 binary bits into 4 levels.
(0,0) maps to level 0
(0,1) maps to level 1
(1,1) maps to level 2
(1,0) maps to level 3

Host Interface: A host interface is defined as the high-speed electrical interface between the module and the host system. The requirements of a specific host interface are defined in the associated industry standard for that interface. See Section 6.1 for use cases.

ISI: A form of signal distortion where one symbol interferes with subsequent symbols is refered as Inter Symbol Inteference (ISI).

Lane: A generic term for the elements associated with transport of one of the high speed signals in one of the module interfaces.

Lower Memory: The 128 bytes addressed by byte addresses 00h through 7fh.

Media Interface: A media interface is defined as the high-speed interface between the module and the interconnect medium, such as wires or optical fibers. The requirements of a specific media interface are defined in the associated industry standard for that interface. See Section 6.1 for use.

Module: Pluggable transceivers and active or passive cable assembly terminations that plug into the host receptacle such as, but not limited to, those of QSFP-DD, OSFP, COBO, QSFP, and SFP-DD form factors - hereafter referred to as modules unless cable assemblies are specifically mentioned.

NV: Non-Volatile memory: a type of memory that can retrieve stored information even after having been power cycled.

OM2: cabled optical fiber containing 50/125 um multimode fiber with a minimum overfilled launch bandwidth of 500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as IEC 60793-2-10 Type A1a.1 fiber.

OM3: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 1500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 2000 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.2 fiber.

OM4: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.3 fiber.

OM5: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm, 1850 MHz-km at 953 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm and 2470 MHz-km at 953 nm in accordance with IEC 60793-2-10 Type A1a.4 fiber.

OMA: Optical Modulation Amplitude: The difference between two optical power levels, of a digital signal generated by an optical source, *e.g.,* a laser diode.

OSNR: Optical Signal to Noise Ratio: The ratio between the optical signal power in a given signal bandwidth and the noise power in a given noise reference bandwidth.

Page: A management memory segment of 128 bytes that can be mapped into Upper Memory.

Pave: Average Power: The average optical power

Port: A point of signal entry or signal exit at the module boundary.

Port Function: The functions and resources within the module that process an signal before leaving and after entering the module through a module port.

Post-cursor equalization: Rx output (module electrical output) setting that reduces post-cursor ISI.

Pre-cursor equalization: Rx output (module electrical output) setting that reduces pre-cursor ISI.

Pulse Amplitude Modulation, four levels (PAM4): a modulation scheme where two bits are mapped into four signal amplitude levels to enable transmission of two bits per symbol.

Rx: an electronic component (Rx) that converts an input signal (optical or electrical) to an electrical (retimed or non-retimed) output signal.

SNR: Signal to Noise Ratio: The ratio of signal power to the noise power, expressed in decibels

tNACK: Time required for the module to accept a single or sequential write to volatile memory.

tWR: Time required to complete a single or sequential write to non-volatile memory.

Tx: a circuit (Tx) that converts an electrical input signal to a signal suitable for the communications media (optical or electrical).

Upper Memory: The 128 bytes addressed by byte addresses 80h through ffh.

4 Introduction and General Description

As a management interface specification the SFP-DD MIS defines the management interface and associated protocols for all required and allowable management interactions between a SFP-DD MIS aware host and a SFP-DD MIS compliant module that are relevant for the host using the module in an application.

4.1 SFP-DD MIS Compliant Modules

SFP-DD MIS Compliant Modules Symmetry is expected between the Tx and the Rx hardware structure; for example Tx lanes that are multiplexed in the Tx are demultiplexed in the Rx. Each Application selected by the host is applied to the same Tx and Rx host electrical lanes.

4.2 Management Protocol Layers

The management interface is best understood in terms of its protocol layers:

- The physical interconnection layer is the lowest layer comprising the electrical and mechanical interface elements (that are required to carry elementary signals) as well as the associated protocols for using those elements.

- The basic management data transfer layer provides the protocols required to let the host and the module exchange elementary management operations (and associated data) via the physical interconnection layer. The basic management operations in SFP-DD MIS are reading and writing bytes from or to a 256-byte addressable memory window. The mechanisms and protocols pertinent to this layer are defined in section 5. Extensions required to effectively address a larger management memory space are described in section 7.

- An optional management message exchange layer can be implemented on top of the basic management data transfer layer and provides primitives for management message exchange between host and module.

- The management application layer specifies the effects of management operations, be it memory registers or messages exchanged, on function or behavior of the module as well as any associated behavioral protocols. This layer is described in sections 6 and 7.

5 Management Interface

The physical layer of the management interface between host and module consists of a serial communication interface and a small set of discrete hardware signals.

5.1 Management Control Signals

The following discrete hardware signals are required by the SFP-DD MIS:

- **IntL/TxFaultDD** - a module signal output on pad 22 set by default to IntL but through TWI can be configured into TxFaultDD indicating laser eye safety or other safety hazards on lane 2.
- **LPMode -** a signal allowing the host to control full or partial power up of the module and pad 25
- **ResetL** - a signal allowing the host to request a complete module reset and on pad 26
- **RxLOS** - an optical signal level indicator for optical lane 1 and outputted on pad 8
- **RxLOSDD** - an optical signal level indicator for optical lane 2 (when exist) and outputted on pad 28
- **TxDisable** - a signal input allowing the host to tunoff module transmitter lane 1, on pad 3. An application that uses both module lanes then TxDisable will turnoff both module transmitter(s) if exists.
- **TxDisableDD** - a signal input allowing the host to tunoff module transmitter lane 2, on pad 23
- **TxFault** - a module output signal on pad 2 indicating laser eye safety or other safety hazards on lane 1 and 2. If IntL/TxFaultDD is configured into TxFaultDD then fault conditions on lane 2 go to pad 22 and pad 2 will indicate fault on lane 1.

SFP-DD control signals are mapped to form factor dependent signals in Appendix A

5.2 Management Communication Interface

5.2.1 General Description

The management communication interface provides a number of elementary management operations that allow the host to read from or write to byte-sized management registers in the management memory map of the module. There are read and write operations both for single bytes and for contiguous byte sequences. Two types of read operations, either with implicit addressing (read from current address) or with explicit addressing, are supported.

The management communication interface distinguishes a **master** role and a **slave** role. The host shall be the master and the module shall be the slave.

The master initiates all operations that lead to data transfer. Data can be transferred from the master to the slave (in write operations) and from the slave to the master (in read operations).

The management communication interface is assumed to be a point-to-point connection.

5.2.2 Physical Layer

The physical layer supporting communication between host and module is the Two Wire serial Interface (**TWI**). The TWI consists of a clock signal (**SCL**) and a data signal (**SDA**).

The master drives the SCL signal to clock data and control information onto the TWI bus. Both master and slave shall latch the state of SDA on the positive transitioning edge of SCL. The host shall initially use a 0-400 kHz SCL clock speed. If a higher management interface speed is supported by the module (see appropriate Hardware Specification) the host may later switch to the faster 0-1 MHz SCL clock speed.

The SDA signal is bi-directional. During binary data transfer, the SDA signal shall transition when SCL is low. SDA transitions when SCL is high are used to mark either the beginning (**START**) or ending (**STOP**) of a data transfer.

Both control bytes and data bytes are transferred bit-serially over the SDA. A LOW voltage encodes 0. A HIGH voltage encodes 1.

The associated protocol to implement the elementary management operation (as byte transfers) over the TWI bit-serial communication link is described in detail in the remainder of this section.

Electrical specifications and TWI timing specifications are found in the appropriate hardware/module specification.

5.3 Serial Communication Protocol

A serial communication protocol over the TWI bus is used to implement management register access operations.

5.3.1 Basic Definitions

5.3.1.1 Start Condition (START)

A high-to-low transition of SDA with SCL high is a START condition.
All TWI bus operations begin with a START condition generated by the master.

5.3.1.2 Stop Condition (STOP)

A low-to-high transition of SDA with SCL high is a STOP condition.

All regular TWI bus operations end with a STOP condition generated by the master.

5.3.1.3 Word Size (Byte)

The TWI word size is 8-bits. TWI words are transferred bit-serially with the most significant bit (MSB) first.

Note: The following text uses the term byte to refer to 8-bit words.

5.3.1.4 Basic Operation Encoding (Control Byte)

The generic TWI address byte is also used to carry a control bit indicating the type of basic management operation. TWI address 10100001b (A1h) indicates a read operation. TWI address 10100000b (A0h) indicates a write operation.

In this specification, the TWI address values 10100001b (A1h) and 10100000b (A0h) are also referred to as a write control byte and read control byte, respectively.

5.3.1.5 Acknowledge (ACK)

After sending a byte, the side driving the TWI bus releases the SDA line for one bit time. During this period the receiving side of the TWI bus pulls SDA low (zero) in order to acknowledge (**ACK**) that it has received the byte.

Not pulling the SDA low in this period is interpreted as a negative acknowledge (**NACK**).

The slave shall ACK each individual control byte received during a read or write operation, and it shall ACK each individual data byte received during a write operation.

The master shall ACK each individual data byte received during a read operation, except for the last data byte, where it terminates the read operation by sending a NACK and STOP.

5.3.1.6 Clock Stretching

To extend the TWI data transfer the slave may pull the clock SCL low. This pull down shall be initiated only while SCL is low. This mechanism can be used by the slave to delay completion of the current basic operation.

5.3.1.7 Acknowledge Polling

After a properly terminated write operation, the slave is allowed to disable its inputs in order to internally realize and finalize the write operation.

Apart from specified maximum durations, the master does not know when exactly the slave is ready to accept the next basic management operation. In this situation the master can use the following acknowledge polling procedure to initiate the next basic management operation as soon as the slave is ready to accept it.

When the slave does not ACK the first byte of an operation (the device address), the master can just repeat sending the START condition followed by the first byte of the operation, until the slave eventually ACKs the first byte.

5.3.2 Protocol Reset and Recovery

5.3.2.1 Power On Reset

The interface shall enter a reset state upon application of power.

5.3.2.2 Protocol Reset and Recovery

Synchronization issues may cause the master and slave to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The TWI protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA.

1. The master shall provide up to a maximum of nine SCL clock cycles (drive low, then high) to the slave
2. The master shall monitor SDA while SCL is high on each cycle.
3. On any clock cycle, if the slave releases SDA, the master shall initiate a STOP condition. The master is then free to send a START condition for the next operation
4. If SDA remains low after nine clock cycles the TWI protocol reset has failed.

5.3.3 Binary Serial Frame Format for Basic Operations

5.3.3.1 Read/Write Control Byte and Response

After the START condition, the first byte of a TWI bus operation is a control byte consisting of a fixed 7-bit part 1010000b followed by a bit indicating the type of operation: A read operation is requested if this bit is 1 (high), A write operation is requested if this bit is 0 (low).

Upon reception of the control byte the slave asserts the SDA signal low to acknowledge (ACK) receipt.

5.3.3.2 Byte Address and Data

Following the control byte, addresses and/or data are transmitted in units of bytes.

In sequential read or write operations (i.e. when transferring multiple data bytes in one operation) the data bytes are transmitted in increasing byte address order over the TWI.

5.4 Read/Write Operations

5.4.1 Slave Memory Current Byte Address Counter (Read and Write Operations)

The slave maintains an internal current byte address counter containing the byte address accessed during the latest read or write operation incremented by one with roll-over as follows: The current byte address counter rolls-over after a read or write operation at the last byte address of the current 128-byte memory page (127 or 255) to the first byte address (0 or 128) of the same 128-byte memory page.

The current byte address counter is incremented whenever a data byte is received or sent by the slave as part of properly terminated management operation.

There is only one current byte address counter and it will change on every TWI transaction. The current byte address counter remains valid between operations as long as power to the slave is maintained and as long as no protocol violations occur. Upon loss of power to or reset of the module or upon operations not terminated by a Stop condition, the current byte address counter contents may be indeterminate.

5.4.2 Data Coherency

Data coherency for two-byte entities in the module management memory map) can be achieved as follows: The master shall use (sequences of) 2-byte sequential reads (see subsection 5.4.4) to retrieve 2-byte data. The slave shall prevent that the master acquires partially updated 2-byte data during any individual 2-byte sequential read.

Data coherency for retrieving contents from registers larger than two bytes is not guaranteed by the basic TWI R/W operations. However data coherency of the contents of 8 byte registers for certain metrics is supported if the metric is advertised as supported.

Data coherency for 8 byte, gated BER Error Count requirements using TWI: the Host shall use an 8 byte sequential read to retrieve the data; the module shall ensure that the 8 bytes come from a discrete sample. Eight byte coherency may require double buffering of the register data.

Data coherency for other cases requires application level interaction protocols, e.g. CDB messages, that are outside the scope of this document.

5.4.3 Byte Read Operations

5.4.3.1 Current Address Read Operation

The master begins the current address read operation with START and then sends the read control byte (10100001).

The slave sends ACK followed by the byte stored at the address given by the current byte address counter.

The master terminates the operation with NACK and STOP.

The slave increments its current byte address counter after orderly termination of the operation.

		<--- CONTROL BYTE --->																		
MASTER	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
SLAVE										ACK	MSB							LSB		
											<---- DATA BYTE ----->									

Figure 5-1 Module Current Address Read Operation

5.4.3.2 Random Read Operation

A random read operation is implemented as a dummy write operation, followed by a current address read operation.

The dummy write operation is used to load the target byte address into the current byte address counter, from which the subsequent current address read operation then reads. The procedure is as follows:

The master generates a START condition and sends the target byte address after the write control byte (10100000b). The master then generates another START condition (aborting the dummy write) and begins a current address read operation by sending a read control byte (10100001b).

The slave acknowledges each byte received. When the byte address of the dummy write is received, the slave updates the current byte address counter. Since the slave then sees the write operation aborted (i.e. when it receives a START instead of a byte to be written), the current byte address counter is not incremented and so contains the address to be read in the subsequent current address read operation.

The master terminates the operation with NACK and STOP when it has received the requested byte.

The slave increments its current byte address counter after orderly termination of the operation and before accepting a new basic management operation.

		<--CONTROL BYTE -->									<BYTE ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL BYTE -->																		
START	MSB						LSB	READ										NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA BYTE n---->									

Figure 5-2 Module Random Read

5.4.4 Sequential Bytes Read Operation

A sequential read operation is the continuation either of a current address read (see Figure 5-3) or of a random address read (see Figure 5-4).

The master indicates continuation of a reading sequence (i.e. sequential read operation) to the slave by sending an ACK after a data byte received (instead of terminating the operation with NACK and STOP).

When the slave receives an ACK after sending a byte to the master, it increments the current byte address counter and sends the byte that is stored at this address.

The sequential read is terminated when the master sends a NACK and a STOP (instead of an acknowledge ACK).

The slave increments its current byte address counter after orderly termination of the operation and before accepting a new basic management operation.

5.4.4.1 Sequential Read from Current Start Address

		<- CONTROL BYTE -->																
MASTER	START	MSB						LSB	READ									ACK
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK	MSB							LSB	
											<---- DATA BYTE n---->								

									ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA BYTE n+1 --->									<-- DATA BYTE n+x --->									

Figure 5-3 Sequential Address Read Starting at Module Current Address

5.4.4.2 Sequential Read from Random Start Address

		<- CONTROL BYTE -->									<BYTE ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL BYTE -->																	
START	MSB						LSB	READ										ACK
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
									ACK	MSB							LSB	
										<---- DATA BYTE n---->								

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA BYTE n+1 --->									<-- DATA BYTE n+x --->									

Figure 5-4 Sequential Address Read Starting with Random Module Read

5.4.5 Byte Write Operation

The master generates a START condition and sends the write control byte (10100000b). When the slave has responded to the write control byte with ACK, the master sends the target byte address. When the slave has responded to the target byte address with ACK, the master sends the data byte value. When the slave has responded to the data byte value with ACK, the master sends STOP to terminate the write operation. Otherwise the write operation is aborted.

On receipt of the target byte address, the slave immediately updates its current byte address counter. However, the slave begins its internal write cycle of the received data byte to the address in the byte address counter not before the write operation is properly terminated by STOP. The slave eventually increments the current byte address counter before accepting then next basic management operation.

If a START condition is received in place of a STOP condition the slave discards the data byte received and does not increment the current byte address counter.

For writes to non-volatile memory, upon receipt of the proper STOP condition, the slave may enter an internally timed write cycle, with maximum duration tWR, to internal memory. Unless otherwise specified, for writes to volatile memory the slave may enter an internally timed write cycle, with maximum duration tNACK, to internal memory.

Note: See the appropriate Hardware specification for tWR and tNACK timing specifications.

The slave may disable its management interface input during an internally timed write cycle and not respond or acknowledge subsequent commands until the internal memory write cycle is complete.

Note: the TWI 'Combined Format' using repeated START conditions is not supported on write commands.

		<- CONTROL BYTE -->									<BYTE ADDRESS>									<- DATA BYTE ->									
MASTER	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	X	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SLAVE										ACK									ACK									ACK	

Figure 5-5 Module Write Byte Operation

5.4.6 Sequential Bytes Write Operation

The master initiates a sequential write operation of up to eight bytes in the same way as a single byte write, but it then does not send a STOP condition after the first byte. Instead, after the slave acknowledges (ACK) receipt of the first data byte, the master transmits up to seven additional data bytes without transmitting new explicit byte address information or control bytes.

Note: For transfers of data blocks larger than eight bytes see section 5.4.2.

The master terminates the sequential write sequence with a STOP condition, otherwise, the operation is aborted and the results of the sequential write are undetermined.

The master shall not include a mixture of volatile and non-volatile registers in the same sequential write.

The slave shall ACK each byte received. The slave may either store a data byte after sending ACK or it may decide to buffer all bytes of the sequential write operation until the operation is terminated by STOP.

After a properly terminated sequential write operation (STOP received) the slave ensures that the current byte address counter contains the address of the next byte after the last byte written, before accepting then next basic management operation. Otherwise, the value of the current byte address counter is undetermined.

Note: At the end of each 128 byte page, the current byte address counter rolls over to the first byte of that page.

For writes to non-volatile memory, upon receipt of the proper STOP condition the slave may enter an internally timed write cycle, with maximum duration tWR, to internal memory. For writes to volatile memory the slave may enter an internally timed write cycle, with maximum duration tNACK, to internal memory.

Note: See the appropriate Hardware specification for tWR and tNACK timing specifications.

The slave may disable its management interface input during an internally timed write cycle and not respond or acknowledge subsequent commands until the internal memory write is complete.

Note that TWI 'combined format' using repeated START conditions is not supported on sequential write commands.

		<- CONTROL BYTE -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

MSB							LSB		MSB							LSB			
x	x	x	x	x	x	x	x	0	x	x	x	x	X	x	x	x	0		
								ACK									ACK		
<--- DATA BYTE n --->									<--- DATA BYTE n+1--->										

MSB							LSB		MSB							LSB			STOP	
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0			
								ACK									ACK			
<--- DATA BYTE n+2--->									<--- DATA BYTE n+x--->											

Figure 5-6 Module Sequential Write Operation

5.5 Timing Specifications

Timing specifications for TWI operations are found in the appropriate hardware/module specification.

Timing specifications for module functions such as module soft control, status, squelch and disable can be found in the appropriate Module Hardware Specification, or they are either specified or advertised in this document.

6 Core Management Features

The behaviors described in this section are required for all SFP-DD MIS modules, unless otherwise noted.

6.1 Module Management Basics

Typical SFP-DD MIS modules have two interfaces between module internal circuitry and external connectors and systems – a host interface and a media interface.

6.1.1 Host Interface Conventions

The host interface is defined as the high-speed electrical interface between the module and the electrical connector in the host system. The host interface consists of signals that travel from the host into the module, referred to as transmitter input signals, and signals that travel from the module into the host, referred to as receiver output signals. All host interface signals are carried between the host and module over electrical differential pairs called host lanes.

6.1.2 Media Interface Conventions

The media interface is defined as the high-speed interface between the module and the interconnect medium, such as wires or optical fibers. The media interface consists of signals that travel from the module into the media, referred to as transmitter output signals, and signals that travel from the media into the module, referred to as receiver input signals. Each unique media interface signal, whether conveyed over a differential pair of electrical wires or an optical wavelength on a physical fiber, is called a media lane.

6.1.3 Interface Memory Map Representations

A set of registers is associated with each interface to control and report status for signals at that interface. All references to host lanes or media lanes in this document refer to the respective registers that control or describe those signals. When the term 'lane' is used without reference to 'host' or 'media' in this specification, a host lane perspective is assumed.

In many cases, module resources are associated with host interface lanes or media interface lanes as a specification convenience, even though the resource may not be physically proximate to the associated interface.

6.2 Module Functional Model

The following sections define functional aspects common to all SFP-DD MIS modules, unless otherwise noted.

6.2.1 Functional Module Capabilities – Applications

The module uses Applications to advertise the set of industry standards that it supports. An Application is defined as a combination of an industry standard host interface and an industry standard media interface. These standards define all necessary attributes for the respective interface, including the signaling baud rate, the signaling modulation format and the number of lanes. A module may support multiple different Applications and/or multiple instances of the same Application.

An Application consists of one or more host electrical lanes and one or more module media lanes. The module advertises the lane or group of lanes onto which an instance of an Application can be assigned. The lane or group of lanes supported by the instance of the Application are identified by the lowest numbered lane in that instance. This identification is advertised for both the host electrical and module media interfaces. Within each instance of an Application, all lanes shall be numbered consecutively on both interfaces, starting with the advertised lowest lane number.

A module may advertise support for a single Application. For example, a module advertises an Application that consists of a 100GAUI-2 host electrical interface and a 100GBASE-SR2 media interface combination.
A module may also advertise support for multiple Applications. For example, a module advertises an Application that consists of a 50GAUI host electrical interface and a 50GBASE-SR media interface combination, and a second Application that consists of a 50GAUI host electrical interface and a 50GBASE-SR media interface combination. The host may select one instances of the first Application or two instances of the second Application. Each instance of each selected Application is independent of other Application instances.

For each Application where the module supports multiple Application instances, hosts need to be able to determine which host electrical lane group corresponds to which module media lane group for each possible Application instance in the module. Modules shall associate the Nth host electrical lane group of the Application with the Nth module media lane group for the same Application. This rule is best illustrated by means of an example. A module advertising support for one instance of a 50GAUI to 50GBASE-SR Application must identify the lowest lane number for each instance on both interfaces. As shown in Figure 6-1 for this example, the Application can be assigned starting on host electrical lane 1 or 2. These possibilities are the first and second lane groups. By rule, the first lane group on the media interface in this example, which starts at media lane 1, must correspond to the first lane group on the host interface, which starts on host lane 1. The second lane group on the media interface, which starts on media lane 2, must correspond to the second lane group on the host interface. Therefore, in this example, the module would advertise host electrical lanes 1 or 2 are supported as the lowest numbered host lane for each instance of the Application, and module media lanes 1, and 2 are supported as the corresponding lowest numbered media lanes.

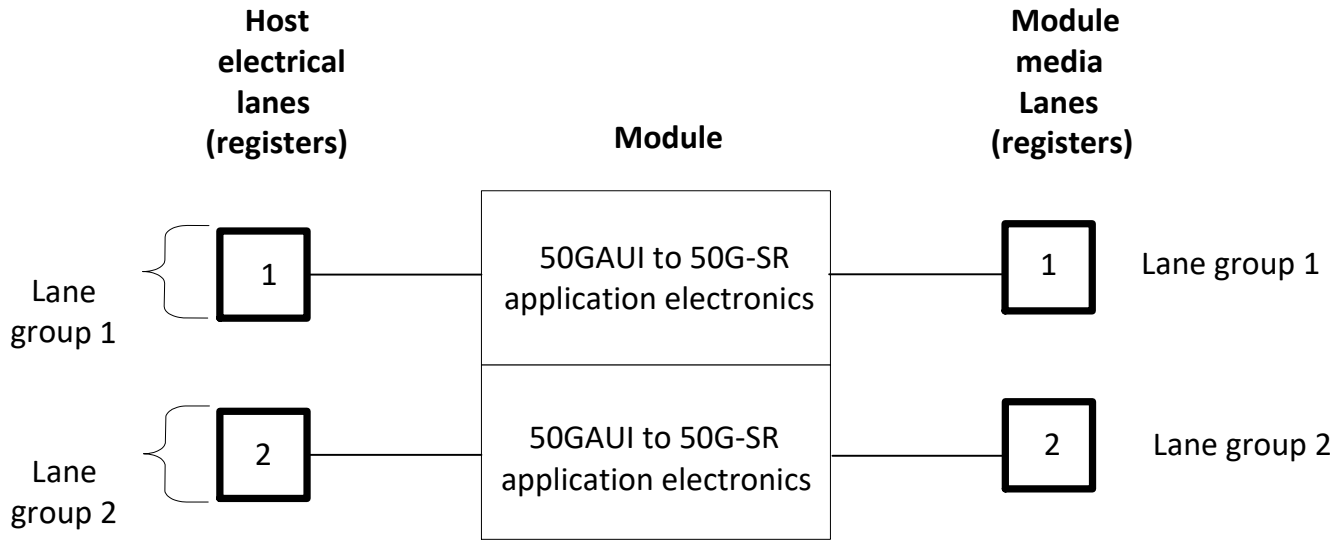

Figure 6-1 Lane Assignment Example

6.2.1.1 Advertising Methodology

The module identifies supported Applications through a set of Application Advertising registers. Within the Application Advertising areas of the memory map, each Application is described by a group of registers, shown in Table 6-1. This specification assigns a unique Application Select code (ApSel code) to each of these register groups. The host uses the ApSel code to select the advertised Application.

In the first byte, the Host Electrical Interface ID identifies the industry standard for the host electrical interface. The list of defined IDs can be found in SFF-8024 where each Host Interface ID is associated with an industry standard, host interface signaling rate, modulation format, and lane count(s). The module defines the maximum supported host interface lane count in the Host Lane Count field, described below. The first unused entry in the table shall be coded FFh to indicate the end of the list of supported Applications.

In the second byte, the Module Media Interface ID identifies the industry standard for the Module Media interface. The list of defined IDs can be found in SFF-8024 Interfaces and Associated IDs in one of the media interface tables. The module identifies which module media interface table applies to the module using the Module Type advertising field in Lower Page 00h Byte 85. The module media interface tables identify the media interface signaling rate, modulation format, and standard-defined lane count(s) for each Module Media Interface ID. The module defines the maximum supported media interface lane count in the Media Lane Count field, described below.

The third byte defines the number of lanes for the host electrical interface and the module media interface. The lane counts shall be consistent with the standards identified in the first and second bytes.

The fourth and fifth bytes identify the lanes where the Application is supported on the host and media interfaces, respectively. The module may support multiple instances of a given Application, so each Lane Assignment Options field identifies the lowest numbered lane in a consecutive group of lanes to which the Application can be assigned. For example, a module supporting two instances of an Application with 50GAUI host interface that can be assigned to Host electrical interface lanes 1 and 2 would advertise a Host Lane Assignment Options value of xxxxxx11b, to indicate that the lowest numbered lane for assignment of an instance of the Application can be lane 1 or lane 2. The fifth byte (Media Lane Assignment Options) identifies where the Application instance is supported on the media interface. The Media Lane Assignment Options register is located on memory map page 01h in Table 7-49, separate from the first four bytes. The Media Lane Assignment Options register is not required for flat memory map modules.

Table 6-1 Module Application Advertising format for one application

Byte	Bits	Name	Description
First	7-0	Host Electrical Interface ID	ID from SFF-8024. The first unused entry in the table shall be coded FFh to indicate the end of the list of supported Applications.
Second	7-0	Module Media Interface ID	ID from SFF-8024. The table to use is identified by the Module Type Encoding in Table 7-23
Third	7-4	Host Lane Count	Number of host electrical lanes 0000b=lane count defined by interface ID (see SFF-8024) 0001b=1 lane, 0010b=2 lanes 0011b-1111b=reserved
	3-0	Media Lane Count	Number of module media lanes. For cable assemblies, this is the number of lanes in the cable. 0000b=lane count defined by interface ID (see SFF-8024) 0001b=1 lane, 0010b=2 lanes...1000b=8 lanes 1001b-1111b=reserved
Fourth	7-0	Host Lane Assignment Options	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit value of 1b indicates that the Application is allowed to begin on the corresponding host lane. In multi-lane Applications each Application shall use contiguous host lane numbers. If multiple instances of a single Application are allowed each starting point is identified. If multiple instances are advertised, all instance must be supported concurrently.
Fifth	7-0	Media Lane Assignment Options	Bits 0-7 form a bit map and correspond to Media Lanes 1-8. A bit value 1b indicates that the Application is allowed to begin on the corresponding media lane. In multi-lane Applications each Application shall use contiguous media lane numbers. If multiple instances of a single Application are allowed each supported starting point is identified. If multiple instances are advertised, all instances must be supported concurrently. This field is not required for flat memory map modules.

This specification provides space for advertisement of up to fifteen Applications. All modules advertise one or more Applications. The module shall advertise the Application used as the power up default in ApSel code 1. The Module Media Interface ID associated with ApSel 1 identifies the common name for the module. The module shall advertise its alternate Applications sequentially starting from ApSel code 2. ApSel codes 1-8 are advertised using Table 7-24.

a. The advertised Application describes the host-media interface combination. It is the module's responsibility to advertise only valid combinations. Hosts shall only select an advertised combination.
b. A module may use the same host interface ID or the same media interface ID in multiple Applications.
c. For cases where a module supports a host electrical interface ID that is included in SFF-8024 but uses a media interface that is proprietary or not yet listed in the media interface advertising ID tables in SFF-8024, the module can use a null ID (00h=undefined) or a custom ID for the media that the module supplier has established, combined with the host electrical interface ID. The host electrical interface ID and lanes provide the required information for the host to interoperate with modules that have unfamiliar or vendor-specific media types and future technologies.

Examples of Application advertising scenarios are shown in Appendix B.

6.2.2 Logical Module Use – Data Paths

The module advertises a list of supported Applications in the Application Advertising Tables described in section 6.2.1.1. The host selects one or more Applications from the advertised options to configure the module for use. When an Application has been selected, the group of module resources that are associated with that Application

instance are collectively referred to as a Data Path. All module resources associated with a Data Path are initialized and deinitialized as a group. Separate Data Paths are initialized and deinitialized independently.

For example, a module advertises an Application that consists of a CAUI host electrical interface and a 100GBASE-SR media interface combination. In this example, the module could advertise support for one or two instances of the Application. Each instance of the Application selected by the host would be a separate Data Path, where each Data Path includes one host electrical lane and one module media lane and is independent of the other Data Path.

In a different example, a module advertises an Application that consists of a 100GAUI-2 host electrical interface and a 100GBASE-DR2 media interface combination, and a second Application that consists of a 50GAUI host electrical interface and a 50GBASE-DR media interface combination. The host may select one instance of the first Application or two instances of the second Application. Each instance of each selected Application becomes a separate, independent Data Path.

6.2.3 Data Path Configuration – Control Sets

A Control Set is a group of registers that are used to provide configuration settings for use by the module during Data Path initialization. Configuration settings are available for each host lane.

The key configuration settings are the Application Select control registers, defined in Table 7-55. These registers allow the host to define one or more Data Paths by mapping desired Applications onto physical lanes in the module. The Application Select control registers include an ApSel code, a Data Path ID and an Explicit Control bit.

Each supported Application advertised in Table 7-24 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific host lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The host lanes used to define a Data Path are a physical reference point for that Data Path but not intended to limit the scope of resources associated with the Data Path. The module resources associated with the Data Path may be located anywhere in the module and may be shared with other host lanes or associated with a media interface in the memory map. An ApSel code of 0000b in an Application Select register indicates that the applicable host lane and its associated resources are not allocated to any data path. When the ApSel code in an Application Select register is 0000b, the Data Path ID and Explicit Control fields in that register may be ignored by the module.

The Data Path ID field in the Application Select control registers is used to specify the lowest numbered host lane in that Data Path. The host shall assign lane combinations that are in accordance with the Lane Assignment Options field advertised by the module for that Application. For a multi-lane data path the host shall write the same Data Path ID in all lanes of that Data Path.

The Explicit Control bit allows the host to indicate that the module should use the host-provided signal integrity values for the resources associated with that lane, instead of using Application-defined signal integrity values. When the Explicit Control bit is programmed as shown in Table 6-2, the associated signal integrity control field value for that lane is used during Data Path initialization. The signal integrity control field value for that lane is ignored for all other values of the Explicit Control bit, and the module shall instead use signal integrity settings that are compliant with the standard associated with the selected Application.

Table 6-2 Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

The usage of these signal integrity control fields is defined in section 6.2.4.

6.2.3.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy settings from Staged Control Set registers into Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests initialization of one or more data paths, the module uses the settings in the Active Control Set to initialize the resources associated with the appropriate data path. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings before exiting the MgmtInit state (see section 6.3.1.6). Module implementers should note that when the Application Select register is programmed to 0000b, that lane has no data path. The module should continue to report a Data Path Status of DataPathDeactivated for such lanes.

There are two controls that can be used to copy the settings from a Staged Control Set to the Active Control Set on a per lane basis: Apply_DataPathInit and Apply_Immediate. When used in the DataPathDeactivated State the Apply_DataPathInit and Apply_Immediate controls only copy the settings into the Active Control Set and do not cause a transition in the Data Path State Machine (see section 6.3.2 for Data Path State Machine details). When the host causes the DataPathDeinitS transition signal to become FALSE (see Table 6-15), the Data Path State Machine shall transition to DataPathInit, regardless of which Apply mechanism had been used.

When used in the DataPathInitialized or DataPathActivated State, the Apply_DataPathInit control copies the Staged Control Set into the Active Control Set and performs a full re-initialization of the data path. In this scenario, the Apply action must be performed on all lanes in the data path at the same time. Use of Apply_DataPathInit in the DataPathActivated state may be disruptive because the Data Path State Machine returns to DataPathInit, where the transmitters are disabled. In cases where new settings need to be applied quickly without disabling the transmitters, such as Fibre Channel Link Speed Negotiation (LSN, see FC FS-6), the host should use the Apply_Immediate control. This control does not transition the Data Path State Machine out of DataPathInitialized or DataPathActivated. Host implementers should note that the host is required to transition the data path state to DataPathDeactivated before the host selects an Application with a different lane count.

The module may report the acceptance or rejection of the requested configuration using the Configuration Error Code registers in Table 7-18. If accepted, the module copies the configuration into the Active Set and changes the data path state. If the configuration is rejected, the module aborts the Apply operation without copying the settings. The Configuration Error Code is reported on all applicable lanes and may differ from data path to data path.

Figure 6-2 illustrates the flow of Control Set settings from the Staged Set into the Active set and module hardware.

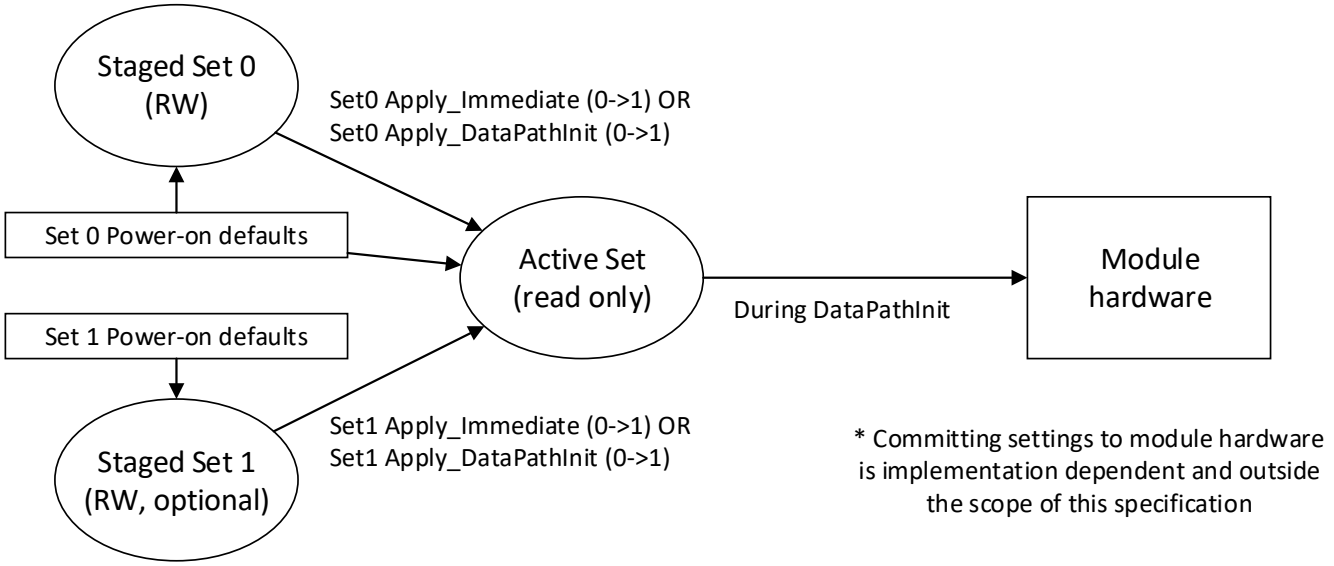

Figure 6-2 Control Set Data Flow Diagram

The translation of memory map settings to the module hardware is implementation-specific and outside the scope of this specification. Module implementers should use a best effort approach when trying to translate memory map settings to module hardware settings.

If the host sets the same bits in both Apply_DataPathInit and Apply_Immediate in the same two-wire serial transaction, the Apply_DataPathInit bit shall take precedence. The host shall not set bits for Apply_DataPathInit or Apply_Immediate when the corresponding data path is in DataPathInit, DataPathDeinit, DataPathTxTurnOn, or DataPathTxTurnOff; the module may ignore such requests.

Host implementers shall adhere to the following rules when using Control Sets:

- The host shall not change the data path width without first transitioning the data path to the DataPathDeactivated state.
- The host shall not Apply staged control set lanes where the Application Select register is set to an ApSel of 0000b unless the associated data path is in the DataPathDeactivated state.
- A valid ApSel shall be assigned to all host lanes in the Active Set at all times
- ApSel = 0000b shall be assigned to each individual unused host lane.

6.2.3.2 Initialization Sequence Examples

The data path architecture described above is intentionally designed to support a broad array of implementations while ensuring compatibility across hosts and modules. Some Applications may not use all of the features provided in the architecture.

Appendix B contains some example host-module initialization flows that can be used for popular Applications.

6.2.4 Signal Integrity Controls

Memory map signal integrity control fields provide a mechanism for the host to override the default signal integrity settings defined by an Application. These signal integrity overrides are only copied to the Active Set (and subsequently committed to module hardware, see Figure 6-2) if the Explicit Control bit is 1 in the applicable Staged Control Set (see Table 7-55 and Table 7-59) when either Apply_DataPathInit on Apply_Immediate is used. If the Explicit Control bit is 0, the module writes the Application-defined default signal integrity values into the

Active Set on an Apply operation. For all signal integrity controls, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

6.2.4.1 Tx Input Equalization Control

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 6-3 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control.

Table 6-3 Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 6-4. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 7-45 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 7-41 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

Table 6-4 Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000b	No Equalization
1	0001b	1 dB
2	0010b	2 dB
3	0011b	3 dB
4	0100b	4 dB
5	0101b	5 dB
6	0110b	6 dB
7	0111b	7 dB
8	1000b	8 dB
9	1001b	9 dB
10	1010b	10 dB
11	1011b	11 dB
12	1100b	12 dB
13-15		Custom

6.2.4.2 Rx Output Emphasis Control

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 7-45 to determine if the module supports Rx Output Emphasis Control. Refer to Table 7-41 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 6-5 Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	No Equalization	No Equalization
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to:

Pre EQ (dB)=-20*log10(1-C(-1)/(C(-1)+C(0)+C(1)))

The post-cursor equalizer settings in dB approximates to:

Post EQ (dB)=-20*log10(1-C(1)/(C(-1)+C(0)+C(1)))

C(n) are equalizer coefficients which are pre-cursor when n is negative and post cursor when n is positive.

6.2.4.3 Rx Output Amplitude Control

The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 7-45 to determine if the module supports Rx Output Amplitude Control and Table 7-41 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows:

Table 6-6 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	Reserved
15	1111b	Custom

6.2.4.4 Tx Input Eq Adaptation Store/Recall Methodology

Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time.

Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 7-45. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient

storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification.

The Tx Input Eq Adaptation Store control field is located in

Table 7-53. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while the data path state is in DataPathInitialized or DataPathActivated and occurs when requested.

The Tx Input Eq Adaptation Recall control field is located in Table 7-56 for Staged Set 0 and Table 7-60 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set.

The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input Eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes.

6.3 Module Behavioral Model

Critical power up and initialization interactions between the host and module are described using state machine behavioral models. These state machines are intended to specify required software behaviors, not software implementation techniques.

Two state machine types are used in this document. A single module-level state machine defines module-wide characteristics, such as the initialization of the management interface and the module power mode. A data path state machine defines the host and module interactions and behaviors needed for initialization of a data path which can be an individual lane or group of lanes in the module. As there can be multiple data paths in the module, there can be multiple data path state machines. For more on data paths see section 6.3.2.

In both module and data path state machines, there are two kinds of states. States where the module is waiting for module hardware or the host to initiate action are referred to as 'steady states'. States that progress to completion without host action are referred to as 'transient states'. In the state machine illustrations, Figure 6-3, Figure 6-4 and Figure 6-5, the steady states have a rectangular outline and the transient states have an oval outline. The durations of steady states are unbounded while the maximum durations of transient states are implementation-dependent and, in some cases, advertised by the module. Dynamic register content may be unreliable during transient states.

This SFP-DD management interface specification leverages the Common Management Interface Specification (CMIS). Therefore, actions and properties are described using generic terms instead of using application-specific signal names. Refer to Appendix A for the association between generic descriptors in this section and application-specific signal names.

6.3.1 Module State Machine

The Module State Machine is used by the module to communicate the availability of module-wide interfaces to the host. Through the Module State Machine, the host can determine when the management interface has completed initialization after power on or on exit from reset. The host can also use the Module State Machine to determine when the high-speed circuitry in paged memory modules is fully powered such that the host can initialize data paths through the Data Path State Machine, described in section 6.3.2.

The Module State Machine is engaged after module insertion and power on. The Module State Machine is applicable to both modules and cable assemblies, whether passive or active. The Module State Machine for devices implementing a paged memory map is described in section 6.3.1. The Module State Machine for devices

implementing a flat (non-paged) memory map is described in section 6.3.1.2. Modules that implement a read-only memory map typically utilize the flat memory model. Modules that implement read-write memory maps should use the paged memory map model.

The Module State Machine describes module-wide behaviors and properties. For data path-specific behaviors and properties, refer to the Data Path State Machine in section 6.3.2.

6.3.1.1 Module State Machine, paged memory modules

Modules that implement a paged memory map shall adhere to the behaviors described by the Module State Machine shown in Figure 6-3.

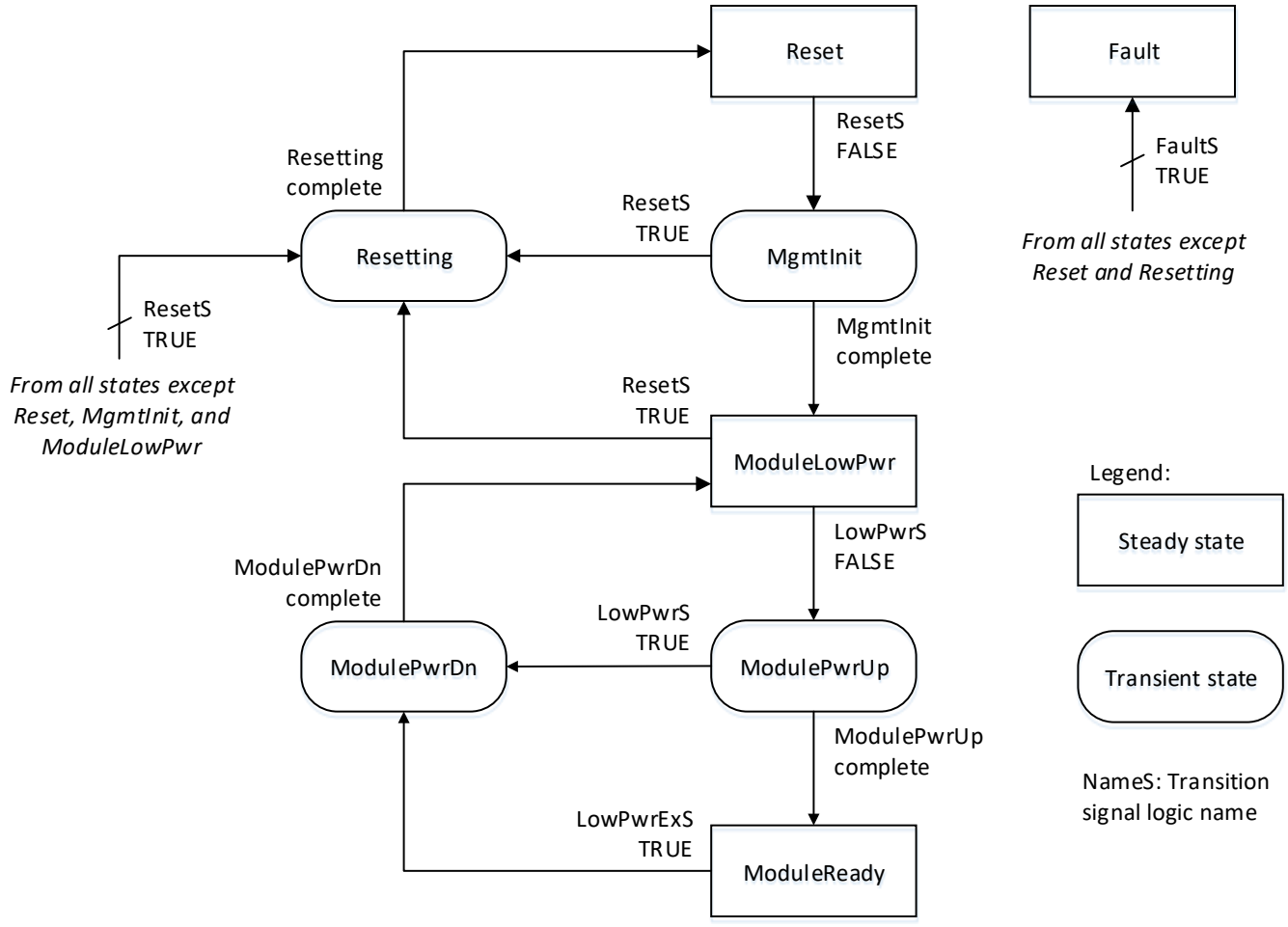

Figure 6-3 Module State Machine, paged memory modules

On module power-up, the Module State Machine is in the Reset state if ResetS is TRUE. Otherwise, the Module State Machine transitions to the MgmtInit state.

The state machine exits a given state when specific conditions are satisfied. Transition signals (names ending in S) are used to summarize a logic condition. The following table describes the priority of exit conditions, if more than one exit condition is satisfied at the same time. Note that not all exit conditions are applicable to all states.

Table 6-7 Module State Machine exit condition priority

Priority	Exit Condition
1	ResetS
2	FaultS
3	All other exit conditions

The ResetS transition signal is described using the truth table shown in Table 6-8, below.

Table 6-8 ResetS transition signal truth table

VccResetL (due to low Vcc)	ResetL hardware signal	Software Reset see Table 7-11	ResetS transition signal
0	X	X	1
1	0	X	1
1	1	1	1
1	1	0	0

The ResetS transition signal can also be represented by the logic equation

ResetS = NOT VccResetL OR NOT ResetL OR Software Reset

VccResetL is defined as the circumstance where the voltage of one or more of the Vcc power rails as observed at the module input drops below an implementation-defined minimum value. Implementation of VccResetL is optional. ResetL, as described in is an active-low signal, and must be asserted for longer than the minimum reset pulse duration to trigger a module reset. Refer to form factor-specific documentation for the minimum reset pulse duration.

The FaultS transition signal truth table and logic equation are module implementation-specific.

The LowPwrS transition signal is described using the truth table shown in Table 6-9, below.

Table 6-9 LowPwrS transition signal truth table

ForceLowPwr see Table 7-11	LowPwr see Table 7-11	LPMode hardware signal	LowPwrS transition signal
1	X	X	1
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

The LowPwrS transition signal can also be represented by the logic equation

LowPwrS = ForceLowPwr OR (LowPwr AND LPMode)

The LowPwrExS transition signal is described using the truth table shown in Table 6-10, below. This transition signal is used to control exit from the ModuleReady state, which occurs when both the LowPwrS transition signal is TRUE and all data paths have reached the DataPathDeactivated state.

Table 6-10 LowPwrExS transition signal truth table

LowPwrS transition signal	Module DeactivatedT	LowPwrExS transition signal
1	1	1
1	0	0
0	1	0
0	0	0

The LowPwrExS transition signal can also be represented by the logic equation

LowPwrExS = LowPwrS AND ModuleDeactivatedT

where

ModuleDeactivatedT = (Lane 1 Data Path State = DataPathDeactivated) AND
(Lane 2 Data Path State = DataPathDeactivated) AND …
(Lane N Data Path State = DataPathDeactivated)
N = number of host lanes in the module

Table 6-11 provides a summary of the high-level behaviors and properties of each module state for paged memory module implementations. Refer to sections 6.3.1.4-6.3.1.11 for detailed requirements for each state.

Table 6-11 Module state behaviors, paged memory modules

State	Power Mode	Behavior in state	Exit condition	Next state	Required/ Optional
Resetting	High/ Low Power	Management interface and all module electronics transition to reset	Resetting completed	Reset	Required
Reset	Low Power	Management interface and all module electronics in reset	ResetS transition signal becomes FALSE	MgmtInit	Required
MgmtInit	Low Power	Management interface powering up and initializing	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			Module management interface ready OR t_init timeout (See Hardware Specification)	ModuleLowPwr	
ModuleLowPwr	Low Power	Management interface available, host may configure module	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			LowPwrS transition signal becomes FALSE	ModulePwrUp	
ModulePwrUp	High Power	Module transitioning to high power mode	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			LowPwrS transition signal becomes TRUE	ModulePwrDn	
			Power up activities are complete	ModuleReady	
ModuleReady	High Power	Module may be consuming power up to the level defined in the fields in Table 7-29	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			LowPwrExS transition signal becomes TRUE	ModulePwrDn	
ModulePwrDn	High Power	Module transitioning to low power mode	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			Module has returned to Low Power mode	ModuleLowPwr	
Fault	*Low Power	Module is waiting for host action	Module power down	N/A	Optional
			ResetS transition signal becomes TRUE	Resetting	

*It is suggested, if possible, that the Fault state be in Low Power mode.

Certain Module State Machine state transitions cause the Module State Changed flag to be set, while other transitions do not set this flag. In general, module-initiated state transitions result in the Module State Changed flag being set. Table 6-12 below defines the appropriate flag behavior for each valid state transition. If the exit criteria for the new state is met upon entry into the state, the Module State Change flag shall not be set. In such

cases, the flag will be set when the Module State completes the multi-step transition sequence, to avoid generation of intermediate state change interrupts to the host.

Table 6-12 Module State Changed flag behaviors

Prior state	Next state	Causes Module State Changed flag to be set?
Fault	Resetting	No
Resetting	Reset	No
Reset	MgmtInit	No
Any state	Resetting	No
Any state	Fault	Yes
MgmtInit	ModuleLowPwr	Yes*
ModuleLowPwr	ModulePwrUp	No
ModulePwrUp	ModuleReady	Yes
ModulePwrUp	ModulePwrDn	No
ModuleReady	ModulePwrDn	No
ModulePwrDn	ModuleLowPwr	Yes

*if the exit condition is not met on entry into the state

6.3.1.2 Module State Machine, flat memory modules

Modules that implement a flat memory map shall adhere to the behaviors described by the Module State Machine shown in Figure 6-4. All other modules shall implement the behaviors described by the Module State Machine for paged memory modules, defined in section 6.3.1.1.

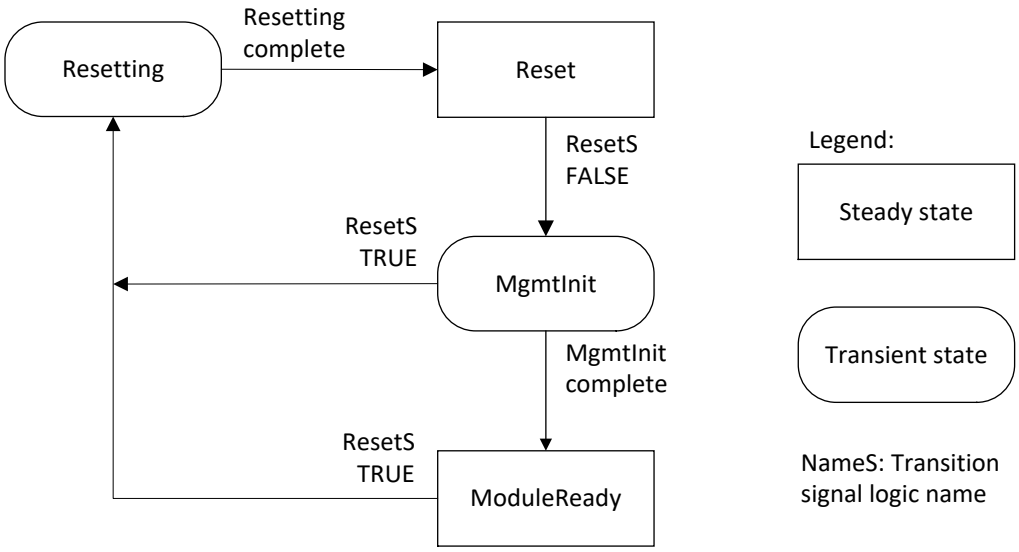

Figure 6-4 Module State Machine, flat memory modules

As shown in Figure 6-4, flat memory modules transition to the ModuleReady state without host interaction. Module state transitions for flat memory modules are a specification formalism, since the contents of the static EEPROM-based memory map does not change. Although the behaviors of the Resetting, Reset, and MgmtInit states apply to such modules, those states are not reported to the host through the memory map. Flat memory modules shall statically advertise a module state of ModuleReady (see Table 7-2).

The ResetS transition signal is described in Table 6-8. For flat memory modules, assertion of the ResetL signal may optionally hold the EEPROM in reset, however the data path shall remain active. Flat memory modules are not required to support Software Reset or VccResetL.

At initial module insertion or application of power, the Module State Machine initializes to the Reset state. Table 6-13 provides a summary of the high-level behaviors and properties of each module state for flat memory modules. Refer to sections 6.3.1.4-6.3.1.11 for detailed requirements for each state.

Table 6-13 Module state behaviors, flat memory modules

State	Power Mode	Behavior in state	Exit condition	Next state	Required/ Optional
Resetting	Low Power	Management interface transitions to reset	Resetting completed	Reset	Optional
Reset	Low Power	Management interface in reset	ResetS transition signal becomes TRUE	MgmtInit	Optional
MgmtInit	Low Power	Management interface powering up and initializing	ResetS transition signal becomes TRUE	Resetting	Required
			Module Management Interface ready AND Interrupt signal asserted OR t_init timeout. (See Hardware Specification)	ModuleReady	
ModuleReady	Low Power	Management interface available	ResetS transition signal becomes TRUE	Resetting	Required

6.3.1.3 Module Power Mode control

The Module Power Mode dictates the maximum power that the module is permitted to consume. The Module Power Mode is a function of the state of the Module State Machine. Two Module Power Modes are defined: Low Power Mode and High Power Mode. The maximum module power consumption in Low Power Mode is defined in the form factor-specific hardware specification. The maximum module power consumption in High Power Mode is module implementation dependent and is advertised in Table 7-29.

All modules initially boot in Low Power Mode, while the module is transitioning through the MgmtInit state. After the management interface has been initialized, the host may transition paged memory modules to High Power Mode using the conditions defined by the LowPwrS transition signal (see Table 6-9). If LowPwrS is FALSE when the module is in the ModuleLowPwr state, the module shall begin power up procedures defined by the ModulePwrUp state (section 6.3.1.8). Conversely, when LowPwrS (or LowPwrExS, as applicable) becomes TRUE, the module begins the transition back to the ModuleLowPwr state and Low Power Mode, using the power down procedures defined by the ModulePwrDn state (section 6.3.1.10).

The LowPwrS transition signal only controls the power mode of the module and not data path initialization. Refer to section 6.3.2 for Data Path State Machine details.

6.3.1.4 Resetting State

The Resetting state is a transient state used by the module to gracefully power down module electronics before entering the Reset state. The Resetting state initiates a complete module reset. The shutdown procedure used by the module for a reset event is implementation dependent. The module may be in High Power Mode during portions of the Resetting state.

The Resetting state is entered from any state except the Reset state when the ResetS transition signal is TRUE. The ResetS transition signal is defined in Table 6-8.

When a paged memory module enters the Resetting state, all Data Path State Machines are torn down. Refer to section 6.3.2 for Data Path State Machine behaviors.

Management interface transactions initiated by the host during the Resetting state may be ignored by the module. Transactions in progress may be aborted when entering the Resetting state. Note: While the ResetS transition signal is TRUE, the management interface may be held in reset and may not respond (NACK).

When all module electronics have been powered down and are in reset, the module state transitions to the Reset state.

6.3.1.5 Reset State

The Reset state is a steady state. The module shall remain in the Reset state as long as the ResetS transition signal is TRUE (see Table 6-8). All internal module electronics shall be placed in reset upon entry into the Reset state for the duration of the state. On entry into the Reset state, the Software Reset bit (Table 7-11) returns to its default value. Note this means that the module hardware implementation must have some mechanism to clear this bit when in the Reset State or upon exiting the Reset State. All other bits are set to their power-up default values in the MgmtInit State, regardless of their value when exiting the Reset State.

The module shall remain in Low Power mode throughout the Reset state. All interrupts shall be suppressed while the module is in the Reset state.

Management interface transactions initiated by the host during the Reset state may be ignored by the module. Transactions in progress may be aborted when entering the Reset state. Note: While the ResetS transition signal is TRUE, the management interface may be held in reset and may not respond (NACK).

After the ResetS transition signal becomes FALSE, the module may not respond until the MgmtInit state is complete. The Reset state can only be exited if the ResetS transition signal is FALSE and power is applied. Upon exit from the Reset state, the module enters the MgmtInit state.

6.3.1.6 MgmtInit State

The MgmtInit state is a transient state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both paged memory modules and flat memory modules.

During this state, the module configures the memory map and initializes the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For paged memory modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state.

Interrupt flag conformance in the MgmtInit state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during MgmtInit.

Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface.

Upon completion of MgmtInit, the next state is ModuleLowPwr.

6.3.1.7 ModuleLowPwr State

The ModuleLowPwr state is a steady state, where the management interface is fully initialized and operational and the device is in Low Power Mode. During this state, the host may configure the module using the management interface and memory map. Some examples of configuration activities include reading the ID and device property fields, setting CDR and other lane attributes and configuration of monitor masks. Details of host-module interactions in the ModuleLowPwr state are implementation dependent and are outside the scope of this specification.

Upon entry into the ModuleLowPwr state, the module shall set the Module State register (Table 7-2) to the ModuleLowPwr state and set the Module State Changed interrupt flag (Table 7-8) only if the ModuleLowPwr exit criteria are not met upon entry into the state. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the ModuleLowPwr state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModuleLowPwr.

The Data Path State for all lanes shall remain in DataPathDeactivated throughout the ModuleLowPwr state.

The module state transitions to ModulePwrUp when the LowPwrS transition signal is FALSE (see Table 6-9). This transition can occur at any time during ModuleLowPwr, and so modules shall regularly sample LowPwrS throughout the ModuleLowPwr state. In some implementations, the LowPwrS transition signal may evaluate to 0 the first time it is sampled in ModuleLowPwr. Host implementers should note that, in such circumstances, the transition to ModulePwrUp may be too fast for the host to detect that the module was in the ModuleLowPwr state.

6.3.1.8 ModulePwrUp state

The ModulePwrUp state is a transient state used to inform the host that the module is in the process of powering up to High Power Mode.

Entry into ModulePwrUp occurs from ModuleLowPwr, when the LowPwrS transition signal is FALSE (see Table 6-9). Upon entry into ModulePwrUp, the module shall set the Module State register (Table 7-2) to the ModulePwrUp state.

The module may be in High Power mode at any time during the ModulePwrUp state.

Interrupt flag conformance in the ModulePwrUp state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModulePwrUp. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

The Data Path State for all lanes shall remain in DataPathDeactivated throughout the ModulePwrUp state.

If the LowPwrS transition signal is TRUE at any time during the ModulePwrUp state, the module state immediately transitions to ModulePwrDn.

When the module power up sequence has completed, the module state transitions to the ModuleReady state.

6.3.1.9 ModuleReady State

The ModuleReady state is a steady state that indicates that the module is in High Power mode. When the module state is ModuleReady, the host may initialize or deinitialize data paths.

Upon entry into the ModuleReady state, the module shall set the Module State register (Table 7-2) to the ModuleReady state and set the Module State Changed interrupt flag (Table 7-8). The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the ModuleReady state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModuleReady.

The only non-Reset or Fault action that results in an exit from ModuleReady is if the LowPwrExS transition signal is TRUE (see Table 6-10), which causes the module state to transition to ModulePwrDn.

6.3.1.10 ModulePwrDn State

The ModulePwrDn state is a transient state that is used to inform the host that the module is in the process of returning to Low Power mode.

Upon entry into the ModulePwrDn state, the module shall set the Module State register (Table 7-2) to the ModulePwrDn state.

The module may be in High Power mode at any time during the ModulePwrDn state.

Interrupt flag conformance in the ModulePwrDn state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModulePwrDn. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

The Data Path State for all lanes shall remain in DataPathDeactivated throughout the ModulePwrDn state.

When the module is in Low Power Mode, the module shall transition to the ModuleLowPwr state. Implementers should note that modules in ModulePwrDn shall ignore the LowPwrS transition signal, so if this signal is FALSE during ModulePwrDn, the module will complete the power-down sequence and transition to ModuleLowPwr before sampling LowPwrS again.

6.3.1.11 Fault State

The Fault state is provided for notification to the host that a module fault has occurred. Definition of the Fault state is implementation dependent. The Fault state shall only be entered when module detects a condition (e.g. laser/eye safety) that could cause damage. The specification intent of the Fault state is to put the module in a condition that does not create further equipment failures. It is recommended that the module enter Low Power mode during the Fault state but the response to a Fault condition is implementation specific. Fault conditions are not maskable.

If the hardware TXFault signal is supported (see Table A-1) it shall report the status of the Fault state. i.e. the TxFault signal is asserted when the module is in the Fault state. When TXFault is asserted the TXDisable is asserted.

The only exit path from the Fault state is to perform a module reset by taking an action that causes the ResetS transition signal to become TRUE (see Table 6-8).

6.3.2 Data Path State Machine

A data path is defined as a combination of one or more host lanes, one or more media lanes, and a set of internal module resources that are collectively identified by a single selected Application. Data paths are only applicable to paged memory modules.

The Data Path State Machine(s) are set-up (come into existence) during MgmtInit, based on the power-up default Application Select field values in the Active Set. The Data Path State Machine(s) are in the DataPathDeactivated

State until the Module State Machine is in the ModuleReady state, and the exit condition from the DataPathDeactivated state is met. Updating the Application Select fields in the Active Set, in either the ModuleLowPwr or ModuleReady states, tears down previous Data Path State Machine(s) that are no longer defined and sets up the newly-defined Data Path State machine(s). All Data Path State Machines are also torn down in the Resetting state.

Refer to section 6.3.1 for an overview of the Module State Machine, section 6.2.1 for an overview of Applications, section 6.2.2 for an overview of Data Paths, and section 6.2.3 for an overview of Control Sets.

The Data Path State Machine is used by the module to communicate the initialization status of the resources associated with a data path. Although individual resources within a data path may complete initialization activities at different times, the module shall wait to report the updated data path state until all resources associated with the data path have completed the requested action. This synchronized status reporting across all lanes and resources in a data path means that there is one Data Path State Machine per data path. This specification describes the behavioral model to be used for each Data Path State Machine. A variety of module implementations that meet this behavioral model are possible but are outside the scope of this specification. Some example data path initialization flows that comply with the Data Path State Machine behavioral model are provided in 0. Modules identify supported data path configuration options through the Application advertisement fields.

Each data path is required to operate independently of other data paths: if the host changes the Data Path State of one data path, the other data paths in the module shall be unaffected and uninterrupted. Module implementers should note that independent operation of data paths may require independent clocking per data path, from a recovered clock within that data path. See the applicable hardware specification for further information. The module shall only advertise Applications and lane configurations that are supported by the implemented clocking scheme. Figure 6-5 shows the Data Path State Machine for one data path instance.

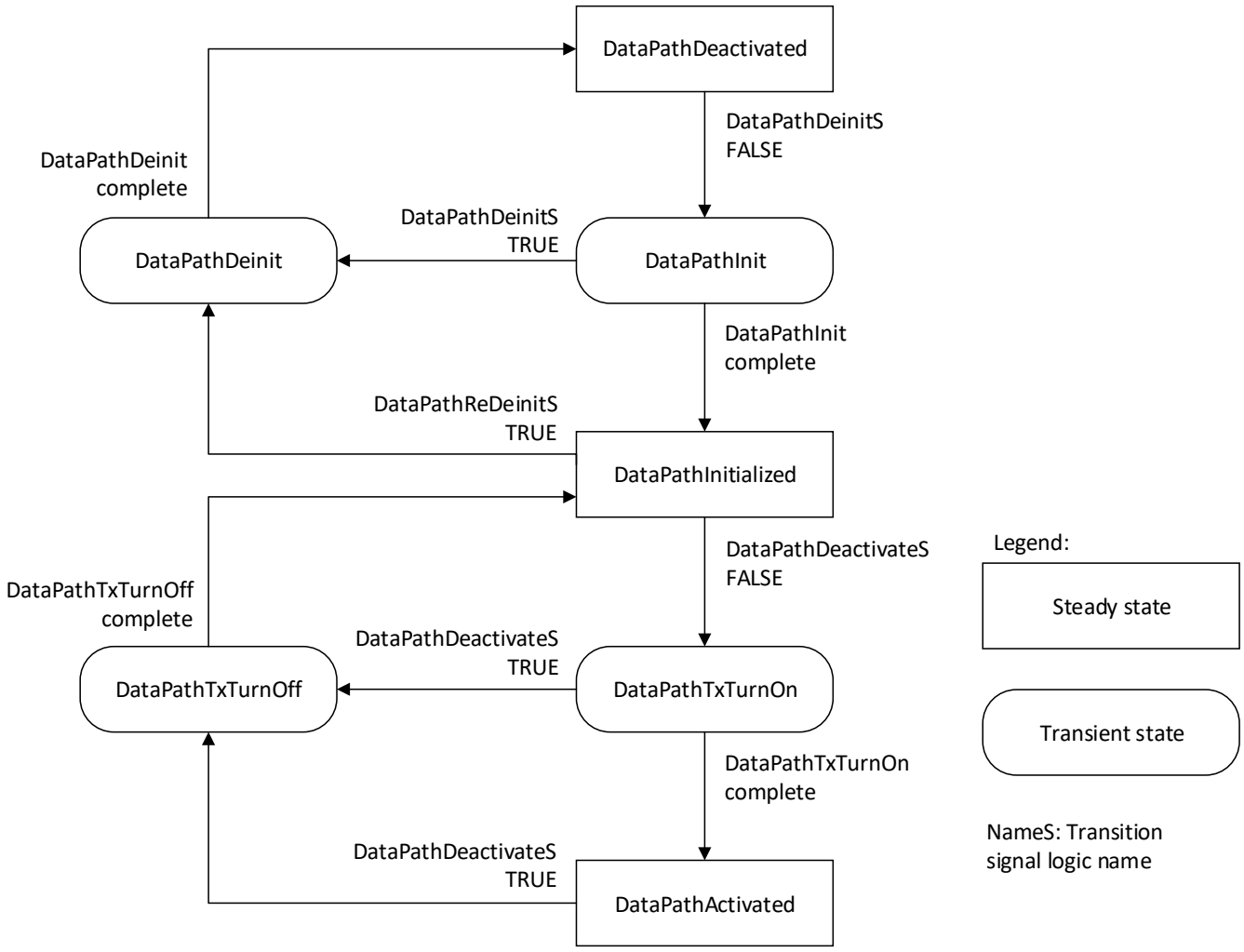

Figure 6-5 Data Path State Machine

The Data Path State Machine describes data path-specific behaviors and properties. For module-wide behaviors and properties, refer to the Module State Machine in section 6.3.1.

Prior to exit from the MgmtInit module state, all data paths initialize to the DataPathDeactivated state.

The state machine exits a given state when specific conditions are satisfied. Transition signals (names ending in S) are used to summarize a logic condition. The following table describes the priority of exit conditions, if more than one exit condition is satisfied at the same time. Note that not all exit conditions are applicable to all states.

Table 6-14 Data Path State Machine exit condition priority

Priority	Exit Condition
1	ResetS
2	FaultS
3	All other exit criteria

The DataPathDeinitS transition signal is described using the truth table shown in Table 6-15, below.

Table 6-15 DataPathDeinitS transition signal truth table

ModuleReadyT	LowPwrS see Table 6-9	DataPathDeintT	DataPathDeinitS transition signal
0	X	X	1
1	1	X	1
1	0	1	1
1	0	0	0

The DataPathDeinitS transition signal can also be represented by the logic equation

DataPathDeinitS = NOT ModuleReadyT OR LowPwrS OR DataPathDeinitT

where

ModuleReadyT = (Module State = ModuleReady)
DataPathDeinitT = (DataPathDeinit Lane N) OR
(DataPathDeinit Lane N+1) OR …
(DataPathDeinit Lane N+M-1)
N = first host lane in the data path
M = number of host lanes in the data path

The DataPathReDeinitS transition signal is described using the truth table shown in Table 6-16, below.

Table 6-16 DataPathReDeinitS transition signal truth table

DataPathDeinitS transition signal	DataPathReinitT	DataPathReDeinitS transition signal
1*	1*	1
1	0	1
0	1	1
0	0	0

*DataPathDeinitS and DataPathReinitT cannot be 1 at the same time

The DataPathReDeinitS transition signal can also be represented by the logic equation

DataPathReDeinitS = DataPathDeinitS OR DataPathReinitT

where

DataPathReinitT = (Lane N Apply_DataPathInit) OR
(Lane N+1 Apply_DataPathInit) OR …
(Lane N+M-1 Apply_DataPathInit)
N = first host lane in the data path
M = number of host lanes in the data path

The DataPathDeactivateS transition signal can be represented by the logic equation

DataPathDeactivateS = DataPathReDeinitS OR DataPathTxDisableT OR DataPathTxForceSquelchT

where

DataPathTxDisableT = (TxN Disable) OR
(TxN+1 Disable) OR …
(TxN+M-1 Disable)
DataPathTxForceSquelchT = (TxN Force Squelch) OR
(TxN+1 Force Squelch) OR …
(TxN+M-1 Force Squelch)
N = first media lane in the data path
M = number of media lanes in the data path

Implementers should note that disabling or forcing squelch on one lane in a data path will cause the entire data path to transition to DataPathInitialized. Although some lanes may continue to be enabled while in DataPathInitialized, since not all lanes are enabled, the data path is considered not activated.

Table 6-17 provides a summary of the high-level behaviors and properties of each data path state. Refer to sections 6.3.2.2-6.3.2.8 for detailed requirements for each state.

Table 6-17 Data path state behaviors

State	Tx output state	Exit condition	Next State
DataPathDeactivated	Quiescent	DataPathDeinitS transition signal becomes FALSE	DataPathInit
DataPathInit	Quiescent	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathDeinitS transition signal becomes TRUE	DataPathDeinit
		Module completes data path initialization	DataPathInitialized
DataPathInitialized	Depends on per-lane Tx Disable and Tx Force Squelch	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathReDeinitS transition signal becomes TRUE	DataPathDeinit
		DataPathDeactivateS transition signal becomes FALSE	DataPathTxTurnOn
DataPathDeinit	Quiescent	ResetS transition signal becomes TRUE	DataPathDeactivated
		Data path deinitialization complete	DataPathDeactivated
DataPathTxTurnOn	In transition	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathDeactivateS transition signal becomes TRUE	DataPathTxTurnOff
		Module Tx output is enabled and stable	DataPathActivated
DataPathActivated	Enabled	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathDeactivateS transition signal becomes TRUE	DataPathTxTurnOff
DataPathTxTurnOff	In transition	ResetS transition signal becomes TRUE	DataPathDeactivated
		Module Tx output is squelched or disabled	DataPathInitialized

The Rx output state is not controlled by the Data Path State Machine. The host may control the Rx output using the Rx Output Disable control (Table 7-53).
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As shown in Figure 6-5, if the ResetS transition signal (see Table 6-8) becomes TRUE during any state, the data path state transitions to DataPathDeactivated without transitioning through DataPathDeinit. In this scenario, any data path-specific power down activities should be performed as part of the Resetting module state.
Certain Data Path State Machine state transitions shall cause the Data Path State Changed flag to be set, while other transitions shall not set this flag. In general, module-initiated state transitions result in the Data Path State Changed flag being set. Table 6-18 below defines the appropriate flag behavior for each valid state transition.

Table 6-18 Data Path State Change flag behaviors

Prior state	Next state	Causes Data Path State Changed flag to be set?
DataPathDeactivated	DataPathInit	No
DataPathInit	DataPathInitialized	Yes*
DataPathInit	DataPathDeinit	No
DataPathInit	DataPathDeactivated	(on ResetS) No
DataPathInitialized	DataPathDeinit	No
DataPathInitialized	DataPathDeactivated	(on ResetS) No
DataPathDeinit	DataPathDeactivated	Yes*
DataPathTxTurnOn	DataPathActivated	Yes
DataPathTxTurnOn	DataPathTxTurnOff	No
DataPathTxTurnOn	DataPathDeactivated	(on ResetS) No
DataPathActivated	DataPathTxTurnOff	No
DataPathActivated	DataPathDeactivated	(on ResetS) No
DataPathTxTurnOff	DataPathInitialized	Yes*
DataPathTxTurnOff	DataPathDeactivated	(on ResetS) No

*if the exit condition is not met on entry into the state

There are circumstances when steady state exit conditions are already met upon entry into the state. An example of this scenario is a data path reinitialization that is triggered when the data path is in DataPathActivated. In this example, the Data Path State Machine transitions through every data path state as it makes the data path transmitter outputs quiescent, deinitializes the existing data path, initializes the new data path, and re-enables the transmitters. The module shall only set the Data Path State Complete flags once, when all chained state transitions have completed.

To facilitate understanding of this mechanism, this specification defines a variable called DataPathStateChangeFlagNeededV. This variable is for specification purposes only and is not reported in the memory map. The DataPathStateChangeFlagNeededV specification variable is per host lane and all lanes are initialized to 0 during the MgmtInit module state. This variable is updated in each transient data path state, depending on the advertised MaxDuration for that state. Once the final steady state in the chain is reached, if the DataPathStateChangeFlagNeededV variable is non-zero, the Data Path State Change Flag bit for that lane is set to 1.

6.3.2.1 Data Path control and status

A single register is provided for the host to control initialization and deinitialization of all data paths in a given bank. This register, called DataPathDeinit, is defined per host lane, to allow flexibility for a variety of data path configurations from a single memory map specification. When the host is requesting initialization or deinitialization of a data path, the host shall write the same value to all DataPathDeinit bits corresponding to all lanes in the applicable data path. The host may request initialization or deinitialization of multiple data paths with one TWI transaction.

The Data Path state register (Table 7-4) defines the current Data Path State for each data path in the module. The module reports the same Data Path State on all lanes in the data path. This synchronized state change behavior means the host only has to read the first lane of the data path to determine the data path state. Although the data path state machine behavioral model described in this specification describes a single state machine per data path, module software implementers may choose to write their software in a variety of ways and still meet the behavioral data path requirements. Some informative data path initialization flows are provided in Appendix B to facilitate understanding of the relationship between the initialization of physical structures in the module and data path-level reporting in the memory map.

6.3.2.2 DataPathDeactivated State

The DataPathDeactivated state is a steady state that indicates to the host that no data path is initialized on the indicated lane(s). The host may configure or reconfigure data paths on lanes that are reporting the DataPathDeactivated state in the Data Path State register (Table 7-4).

DataPathDeactivated is entered when any of the following conditions occur

a. The ResetS transition signal is TRUE (Table 6-8).
b. The module exits the Reset module state, for example on module insertion.
c. Any data path completes the DataPathDeinit state.

Upon entry into the DataPathDeactivated state, the module sets the Data Path state register (Table 7-4) for all lanes in the applicable data path(s) to DataPathDeactivated. If the exit conditions for DataPathDeactivated are not satisfied immediately on entry into the state, the module sets the Data Path State Change flag (Table 7-6) to 1 on each lane where the DataPathStateChangeFlagNeededV specification variable is non-zero before clearing DataPathStateChangeFlagNeededV for that lane. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

All transmitter outputs associated with the data path in DataPathDeactivated shall be quiescent throughout the state. Changes to Tx disable or squelch for data paths in DataPathDeactivated shall have no impact on the output quiescence of those data path.

Interrupt flag conformance in the DataPathDeactivated state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathDeactivated.

The Data Path State Machine shall only transition to DataPathInit when the DataPathDeinitS transition signal is FALSE (Table 6-15), unless the ResetS transition signal is TRUE (Table 6-8). The data path state shall remain in DataPathDeactivated as long as ResetS is TRUE. The Host shall provide a valid high-speed input signal at the required signaling rate and encoding type prior to the transition to DataPathInit. The host may request initialization of multiple data paths in one request.

6.3.2.3 DataPathInit State

The DataPathInit state is a transient state that indicates that the module is performing initialization activities on the data path. Initialization activities include application of the selected Application properties, application and/or adaptation of signal integrity settings, and optional power up of Tx and Rx data path electronics if opportunistic power savings was employed by the module in DataPathDeactivated. The host shall provide a valid high-speed input signal at the required signaling rate and encoding type prior to entering the DataPathInit state.

Upon entry into the DataPathInit state, the module sets the Data Path state register (Table 7-4) for all applicable lanes to DataPathInit. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathInit_MaxDuration value (Table 7-39). The advertised DataPathInit_MaxDuration includes the time to perform all of DataPathInit activities on all lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathInit state. If the DataPathInit_MaxDuration register is set to 0, the worst-case duration of DataPathInit is less than 1 ms and the module will not report the DataPathInit state in the Data Path State register and may or may not report the completion of the state via the Data Path State Changed flag or Interrupt signal.

Within the DataPathInit state, the module performs any remaining power-up activities for module electronics associated with the data path(s) in DataPathInit. In some cases, these electronics may be shared between multiple data paths. Depending on prior power up and down actions, some or all of these electronics may already be powered; in such cases, the power up sequence is bypassed. The details of the power up sequence are implementation-dependent and outside the scope of this specification.

During DataPathInit, the module shall also apply the selected Application properties in the Active Set (see section 6.2.3) to the applicable data path module resources. The details of how the module applies Application settings is implementation-dependent and outside the scope of this specification. The module shall also apply the signal integrity settings in the Active Set during DataPathInit. Entry into DataPathInit shall trigger a full initialization of all applicable data path(s). For example, attributes that require adaptation, such as CTLE settings, shall be adapted at the appropriate time during DataPathInit. The order in which signal integrity settings are applied and adapted is implementation-dependent and outside the scope of this specification. Implementers should note that no input signal may be present at the module Rx input at the time of initialization. In such cases, the module electronics shall be fully configured, such that any required adaptation or CDR locking occurs automatically at a later point in time when an input signal is provided, without host intervention.

For all data paths in DataPathInit, all Tx outputs shall be quiescent throughout the state. Changes to Tx disable or squelch for data paths in DataPathInit shall have no impact on the output quiescence of those data paths.

The host shall minimize TWI transactions while in this state. Dynamic memory map content may be unreliable while in this state and should not be read or written.

Interrupt flag conformance in the DataPathInit state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathInit. However, the module shall not clear any interrupt flags when exiting the DataPathInit state. Interrupt flags are only cleared when the host reads the flag.

If the DataPathDeinitS logic signal is TRUE at any time during DataPathInit, the data path state shall transition to DataPathDeinit. Otherwise, when the module has completed power-up and initialization of all Tx and Rx resources associated with the data path, and all applicable Tx and Rx flags, alarms, and warnings are valid, the data path state transitions to DataPathInitialized.

6.3.2.4 DataPathInitialized State

The DataPathInitialized state is a steady state. Data paths that are in the DataPathInitialized state are considered fully initialized. However, the output of one or more media lane transmitters whose data path is in DataPathInitialized is either squelched or disabled and so the data path is not ready to transmit live traffic.

Upon entry into the DataPathInitialized state, the module sets the Data Path state register (Table 7-4) for all lanes in the applicable data path(s) to the DataPathInitialized state. If the exit conditions for DataPathInitialized are not satisfied immediately on entry into the state, the module sets the Data Path State Change flag (Table 7-6) to 1 on each lane where the DataPathStateChangeFlagNeededV specification variable is non-zero before clearing DataPathStateChangeFlagNeededV for that lane. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the DataPathInitialized state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathInitialized.

Transmitter output quiescence for data paths in DataPathInitialized is determined per media lane by the setting in the Tx Disable and Tx Force Squelch controls, and the Tx LOS condition of the lane.

If the DataPathReDeinitS transition signal is TRUE at any time during DataPathInitialized, the data path state shall transition to DataPathDeinit. Otherwise, if the DataPathDeactivateS signal is FALSE at any time during DataPathInitialized, the data path state shall transition to DataPathTxTurnOn. Either of these conditions may be met upon entry into DataPathInitialized.

6.3.2.5 DataPathDeinit State

The DataPathDeinit state is a transient state where the module can deinitialize the resources associated with a data path. Deinitialization tasks are implementation dependent but can include tasks such as opportunistic power savings or module software variable clean-up.

DataPathDeinit is entered through either of the following host-initiated actions:

a. The DataPathDeinitS transition signal is TRUE (Table 6-15) while in the DataPathInit state.
b. The DataPathReDeinitS transition signal is TRUE (Table 6-16) while in the DataPathInitialized state.

Upon entry into the DataPathDeinit state, the module sets the Data Path state register (Table 7-4) for all lanes in the applicable data path(s) to the DataPathDeinit state. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathDeinit_MaxDuration value (Table 7-39). The advertised DataPathDeinit_MaxDuration, includes the time to perform all of DataPathDeinit activities on all lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathDeinit state. If the DataPathDeinit_MaxDuration register is set to 0, the worst-case duration of DataPathDeinit is less than 1 ms and the module will not report the DataPathDeinit state in the Data Path State register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

During DataPathDeinit, the module may power down applicable data path electronics for opportunistic power savings. In some cases, electronics may be shared with other data paths that are not in DataPathDeinit or DataPathDeactivated. In such cases, these electronics shall remain powered. Similarly, module implementers may identify certain electronics that require significant power up times. Module implementers may choose to keep these electronics powered even when the host requests data path deinitialization. If the host wants to ensure maximum power savings, the host should initiate a module transition to Low Power Mode by causing the LowPwrS signal to become TRUE.

For all data paths in DataPathDeinit, all Tx outputs shall be quiescent throughout the state. Changes to Tx disable or squelch for data paths in DataPathDeinit shall have no impact on the output quiescence of those data paths.

The host shall minimize TWI transactions while in this state. Dynamic memory map content may be unreliable for lanes in this state and should not be read or written.

Interrupt flag conformance in the DataPathDeinit state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathDeinit. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag or sends a reset signal.

When the module has completed deinitialization activities on all resources associated with the data path, the data path state shall transition to DataPathDeactivated.

6.3.2.6 DataPathTxTurnOn State

The DataPathTxTurnOn state is a transient state where the module enables the Tx output for all media lanes associated with the data path.

Upon entry into the DataPathTxTurnOn state, the module sets the Data Path state register (Table 7-4) for all lanes in the applicable data path(s) to the DataPathTxTurnOn state. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathTxTurnOn_MaxDuration value (Table 7-48). The advertised DataPathTxTurnOn_MaxDuration, includes the time to enable and stabilize the Tx output on all media lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathTxTurnOn state. If the DataPathTxTurnOn_MaxDuration register is set to 0, the worst-case duration of DataPathTxTurnOn is less than 1 ms and the module will not report the DataPathTxTurnOn state in the Data Path State register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

Interrupt flag conformance in the DataPathTxTurnOn state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathTxTurnOn. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag or sends a reset signal.

If the DataPathDeactivateS transition signal becomes TRUE at any time during DataPathTxTurnOn, the data path state transitions to DataPathTxTurnOff. The data path advances to DataPathActivated once all Tx outputs associated with the data path are enabled, have stabilized, and are ready to transmit live traffic.

6.3.2.7 DataPathActivated State

The DataPathActivated state is a steady state. Data paths that are in the DataPathActivated state are considered fully initialized and ready to transmit live traffic.

Upon entry into the DataPathActivated state, the module sets the Data Path state register (Table 7-4) for all lanes in the applicable data path(s) to the DataPathActivated state. If the exit conditions for DataPathActivated are not satisfied immediately on entry into the state, the module sets the Data Path State Change flag (Table 7-6) to 1 on each lane where the DataPathStateChangeFlagNeededV specification variable is non-zero before clearing DataPathStateChangeFlagNeededV for that lane. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the DataPathActivated state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathActivated.

All transmitter outputs associated with the data path in DataPathActivated shall be enabled throughout the state.

The data path state transitions to DataPathTxTurnOff if the host causes the DataPathDeactivateS transition signal to become TRUE for that data path. The host may transition multiple data paths to DataPathDeinit simultaneously.

One way for the DataPathDeactivateS transition signal to become TRUE is if the host sets the Apply_DataPathInit bits associated with the data path to 1. The host may choose to reconfigure one or more data paths while in DataPathActivated by applying a new Application in one of the Staged Control Sets to the applicable data paths using Apply_DataPathInit. The host shall set Apply_DataPathInit to a uniform value for all lanes in the data path being reinitialized. When Apply_DataPathInit bits are set to 1, the data path state will transition through the DataPathTxTurnOff -> DataPathInitialized -> DataPathDeinit -> DataPathDeactivated -> DataPathInit -> DataPathTxTurnOn -> DataPathActivated state sequence, reinitializing the new data path configuration in DataPathInit.
Prior to setting the Apply_DataPathInit bits for applicable lanes, the host shall provide a valid high-speed input signal at the required signaling rate and encoding type. Host implementers should note that the Apply_DataPathInit bits for all lanes in the data path shall be set with one TWI transaction. The host may request reinitialization of multiple data paths in the same TWI transaction. Module implementers should note that data paths excluded from the Apply_DataPathInit lane mask shall not transition Data Path States nor change data path properties. This selective control allows host reconfiguration of individual data paths in breakout Applications without affecting the operation of other data paths in the module.

The DataPathDeactivateS transition signal will also become TRUE if the host writes a 1 to the Tx Disable or Tx Force Squelch lanes associated with the data path during DataPathActivated or if one of those lanes experiences a Tx LOS event and Tx Squelch is supported and enabled.

6.3.2.8 DataPathTxTurnOff State

The DataPathTxTurnOff state is a transient state where the module performs the applicable Tx Disable and/or Tx Force Squelch action on applicable lanes in the data path. This state indicates to the host that the data path is no longer activated and cannot send traffic on all lanes.

Upon entry into the DataPathTxTurnOff state, the module sets the Data Path state register (Table 7-4) for all lanes in the applicable data path(s) to the DataPathTxTurnOff state. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathTxTurnOff_MaxDuration value (Table 7-48). The advertised DataPathTxTurnOff_MaxDuration, includes the time to enable and squelch or disable the Tx output on all media lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathTxTurnOff state. If the DataPathTxTurnOff_MaxDuration register is set to 0, the worst-case duration of DataPathTxTurnOff is less than 1 ms and the module will not report the DataPathTxTurnOff state in the Data Path State register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

Interrupt flag conformance in the DataPathTxTurnOff state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathTxTurnOff. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag or sends a reset signal.

Transmitter output quiescence for data paths in DataPathInitialized is determined per media lane by the setting in the Tx Disable and Tx Force Squelch controls, and the Tx LOS condition of the lane.

The data path advances to DataPathInitialized once the applicable Tx outputs associated with the Tx Enable or Tx Force Squelch action have achieved the requested behavior and have stabilized.

6.3.3 Interrupt Flag Conformance per State

Some flags are generated by the Module or Data Path State Machines, but the majority of flags are triggered by other sources. In some states, certain flags are not applicable and should be inhibited. The following sections define the conformance for all interrupts for each state in the Module and Data Path State Machines.

6.3.3.1 Module Flag Conformance per State

Table 6-19 describes the flag conformance for all module flags, per module state. In module states where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the module is in that state. All module flags shall be 'Not Allowed' throughout the Resetting, Reset, and MgmtInit states. Module flag conformance is not dependent on Data Path State. Some module interrupts are module-configurable; Table 6-19 defines the flag conformance for each configuration option for those flags. Host implementers should note that if certain interrupts are undesirable, the host may mask those interrupts by setting the corresponding interrupt mask bit at any time after the management interface is initialized.

Table 6-19 Module Flag Conformance

Flag	Page	Byte	ModuleLowPwr Alarm	ModulePwrUp ModulePwrDn ModuleReady
Module state change	00h	8	Allowed	Allowed
Module temperature	00h	9	Allowed	Allowed
Vcc 3.3V	00h	9	Allowed	Allowed
Aux1 – TEC Current	00h	10	Not Allowed	Allowed
Vendor-defined	00h	11	See below	Allowed

The vendor-defined flag is Allowed in ModuleLowPwr if and only if it applies to a feature that is available in Low Power Mode.

6.3.3.2 Lane-Specific Flag Conformance per State

Table 6-20 and Table 6-21 describe the flag conformance for all lane-specific flags, per Data Path State. In Data Path States where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the data path is in that state. All lane-specific flags shall be 'Not Allowed' throughout the Reset and MgmtInit module states. For all other module states, implementers should refer to the Data Path State to determine lane-specific flag conformance. Host implementers should note that if certain interrupts are undesirable, the host may mask those interrupts by setting the corresponding interrupt mask bit at any time after the management interface is initialized.

Table 6-20 Lane-Specific Flag Conformance

Flag	Page	Byte	DataPath Deactivated	DataPath Initialized	DataPathInit	DataPathDeinit
Data Path State Change[1]	00h	5	Allowed	Allowed	Not Allowed	Not Allowed
Tx Fault	00h	5	Allowed	Allowed	Allowed	Allowed
Tx LOS	00h	6	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx CDR LOL	00h	6	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Adaptive Input Eq Fail	00h	5	Not Allowed	Allowed	Allowed	Not Allowed
Tx output power High Alarm	00h	8	Allowed	Allowed	Allowed	Allowed
Tx output power Low Alarm	00h	8	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx output power High Warning	00h	8	Allowed	Allowed	Allowed	Allowed
Tx output power Low Warning	00h	8	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High Alarm	00h	9	Allowed	Allowed	Allowed	Allowed
Tx Bias Low Alarm	00h	9	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High Warning	00h	9	Allowed	Allowed	Allowed	Allowed
Tx Bias Low Warning	00h	9	Not Allowed	Allowed	Not Allowed	Not Allowed
Rx LOS	00h	6	Allowed	Allowed	Allowed	Allowed
Rx CDR LOL	00h	6	Not Allowed	Allowed	Not Allowed	Not Allowed
Rx Input Pwr High Alarm	00h	7	Allowed	Allowed	Allowed	Allowed
Rx Input Power Low Alarm	00h	7	Not Allowed	Allowed	Not Allowed	Not Allowed
Rx Input Power High Warning	00h	7	Allowed	Allowed	Allowed	Allowed
Rx Input Power Low Warning	00h	7	Not Allowed	Allowed	Not Allowed	Not Allowed

Note 1: The Data Path State Changed flag is only allowed when the DataPathStateChangeFlagNeededV specification variable is nonzero and the exit conditions for the applicable steady state are not satisfied when the state is entered.

Table 6-21 Lane-Specific Flag Conformance, additional data path states

Flag	Page	Byte	DataPath Activated	DataPath TxTurnOn	DataPath TxTurnOff
Data Path State Change[1]	00h	5	Allowed	Not Allowed	Not Allowed
Tx Fault	00h	5	Allowed	Allowed	Allowed
Tx LOS	00h	6	Allowed	Allowed	Allowed
Tx CDR LOL	00h	6	Allowed	Allowed	Allowed
Tx Adaptive Input Eq Fail	00h	5	Allowed	Allowed	Allowed
Tx output power High Alarm	00h	8	Allowed	Allowed	Allowed
Tx output power Low Alarm	00h	8	Allowed	Allowed	Allowed
Tx output power High Warning	00h	8	Allowed	Allowed	Allowed
Tx output power Low Warning	00h	8	Allowed	Allowed	Allowed
Tx Bias High Alarm	00h	9	Allowed	Allowed	Allowed
Tx Bias Low Alarm	00h	9	Allowed	Allowed	Allowed
Tx Bias High Warning	00h	9	Allowed	Allowed	Allowed
Tx Bias Low Warning	00h	9	Allowed	Allowed	Allowed
Rx LOS	00h	6	Allowed	Allowed	Allowed
Rx CDR LOL	00h	6	Allowed	Allowed	Allowed
Rx Input Pwr High Alarm	00h	7	Allowed	Allowed	Allowed
Rx Input Power Low Alarm	00h	7	Allowed	Allowed	Allowed
Rx Input Power High Warning	00h	7	Allowed	Allowed	Allowed
Rx Input Power Low Warning	00h	7	Allowed	Allowed	Allowed

Note 1: The Data Path State Changed flag is only allowed when the DataPathStateChangeFlagNeededV specification variable is nonzero and the exit conditions for the applicable steady state are not satisfied when the state is entered.

7 Module Management Memory Map

This section defines the register memory map for a SFP-DD MIS compliant module.

7.1 Overview

7.1.1 Memory Structure and Mapping

The TWI protocol defined in section 5.2 only supports eight-bit addresses. This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in **Lower Memory** (addresses 00h through 7Fh) and **Upper Memory** (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory[1] is shown in Figure 7-2. The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (**Pages**), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a **bank** of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

> *Note: The management memory map has been designed largely after the* CMIS *memory map where pages and banks are used in order to enable time critical interactions between host and module while expanding the memory size. This memory map has been changed in order to accommodate just two electrical lanes and to limit the required memory. The single address approach is used as found in QSFP.*

7.1.2 Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all SFP-DD MIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See Table 7-39 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additionally, support for Page 01h is required for all paged memory modules.

Bank 0 of pages 13h-14h, provide diagnostic registers.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages can be implemented to support modules with larger management memory needs.

[1] The actual storage structure of the memory pages is not in the scope of this specification. This specification only defines how the available memory pages can be addressed.

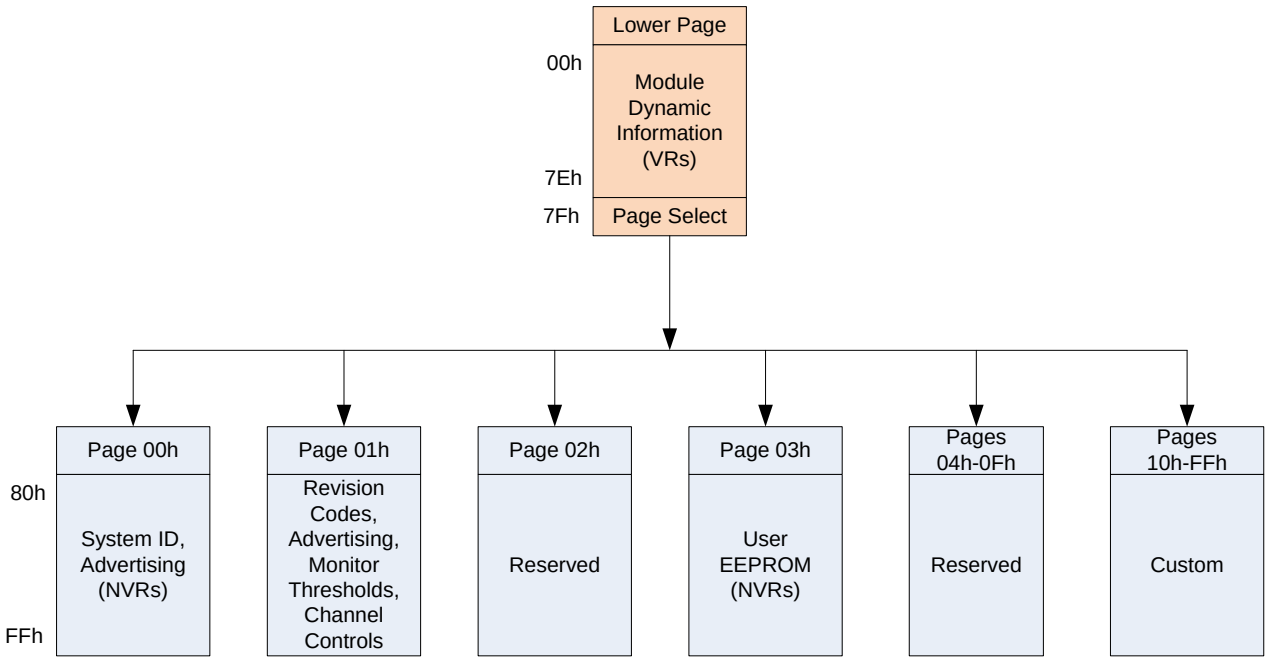


Figure 7-1 SFP-DD MIS Module Memory Map

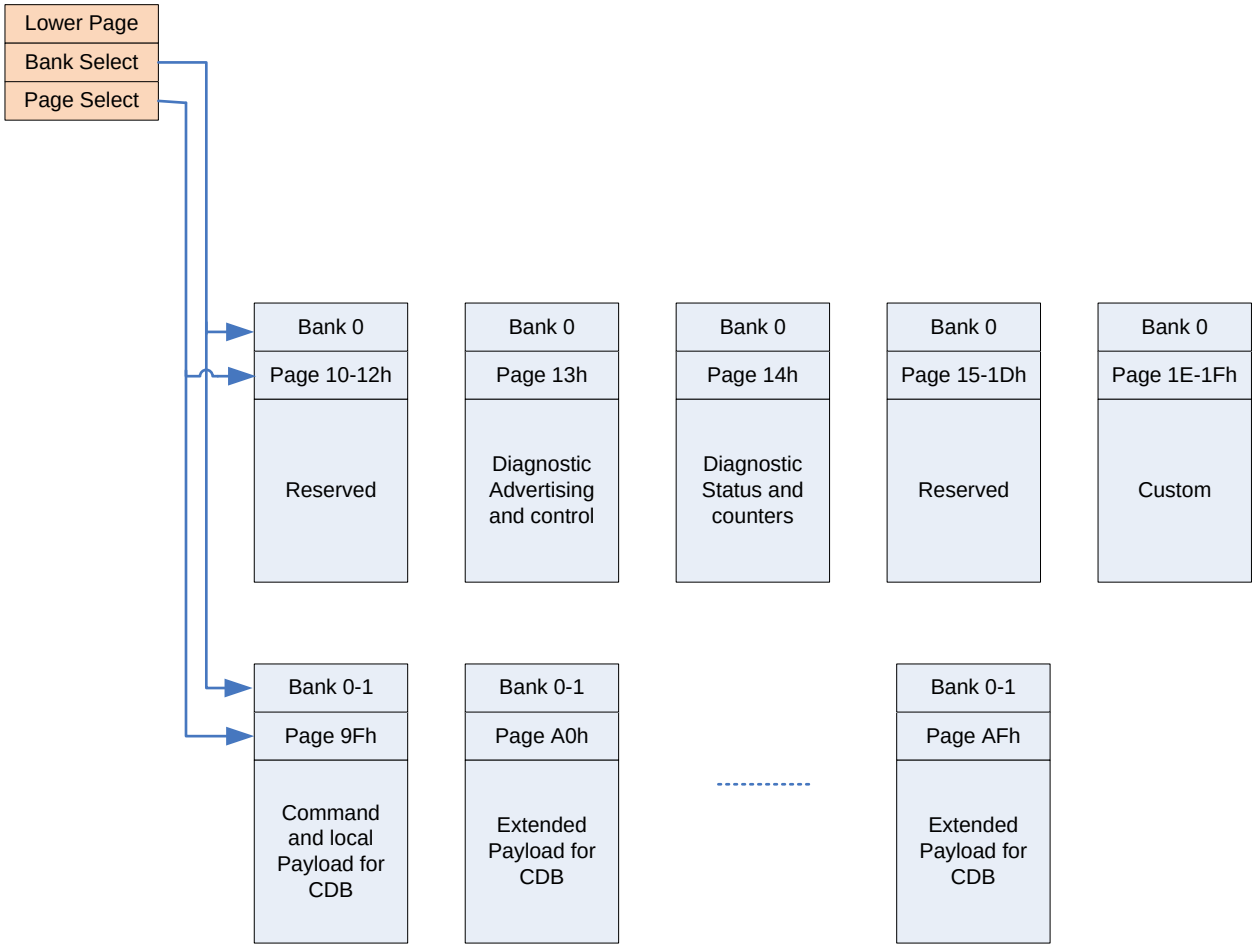


Figure 7-2 SFP-DD MIS Bank Page Memory Map

7.1.3 General Specifications and Conventions

7.1.3.1 Referring to Bytes and Fields

Each byte in the internal management memory can be identified by an address triple consisting of a bank index (0-255), a page index (00h-FFh), and a byte address (0-255). The bank index 0 can be omitted for Pages without bank support. Bank index 0 and page number 00h can be omitted for the Lower Page.

With bits in a byte numbered from 0 to 7 per arithmetic significance, the following notation syntax may be used to identify each bit or bit field:

bank:page:byte.bit
bank:page:byte.bit-bit.

7.1.3.2 Reserved Bytes, Fields, or Bits

Reserved locations (bytes, fields, or bits) are for future use and shall neither be used (evaluated) nor modified. The module shall zero-initialize reserved locations. There are no other obligations for the module. The results of forbidden host writes to reserved locations are undefined.

Other organizations shall contact the managing organization or the editor of this document to request allocations of register bytes, fields, or bits.

7.1.3.3 Custom Bytes or Fields

Custom bytes usage is not restricted and may be vendor defined. The use of registers defined as custom may be subject to additional agreements between module users and vendors.

7.1.3.4 Register Default Values

Default values for all control registers are 0 unless otherwise specified. Host implementers are encouraged to review critical registers and not rely on module default values. For Control Set registers the default settings may be Application dependent, see section 6.2.3.

7.1.3.5 Endian Format

Unless otherwise stated, all multibyte data registers are big endian.

7.2 Lower Memory Page 00h (Control and Status Essentials)

The Lower Memory consists of the lower 128 bytes of the 256 byte two-wire serial bus addressable space.

The Lower Page is used to access a variety of module level measurements, diagnostic functions and control functions, as well as to select which of the various Upper Pages in the structured memory map are accessed by byte addresses greater or equal than 128.

This portion of the 256 byte accessible address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

The lower page is subdivided into several subject areas as shown in the following table:

Table 7-1 Lower Memory Overview

Address	Size	Subject Area	Description
0–3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-9	6	Lane-Level Flags	Flags that are lane or data path specific
10-13	4	Module-Level Flags	All flags that are not lane or data path specific
14-21	12	Module-Level Monitors	Monitors that are not lane or data path specific
22-25	4	Wavelength and Fiber mapping	
26	1	Module Global Controls	Controls applicable to the module as a whole
27-28	2	Reserved	
29-30	2	Custom	
31-36	6	Reserved	
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-52	12	Reserved Area	Reserved for future standardization
53-57	5	Lane Masks	Vendor or module type specific use
58-61	4	Module Masks	
62-73	12	Tx/Rx Power/Bias	
74-82	9	Control Set	
83-84	2	Reserved	
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

7.2.1 ID and Status

The ID and Status fields described in Table 7-2 provide fundamental memory map characteristics (module type, flat or paged memory, memory map version) as well as module status indicators.

Table 7-2 Identifier and Status Summary (Lower Page)

Byte	Bits	Field Name	Description	Type
0	7-0	Identifier	Identifier - Type of Serial Module - See SFF-8024.	RO RQD
1	7-0	Revision Compliance	Identifier – SFP-DD MIS revision; the upper nibble is the whole number part and the lower nibble is the decimal part. Example: 01h indicates version 0.1, 21h indicates version 2.1.	RO RQD
2	7	Flat_mem	Upper memory flat or paged. 0b=Paged memory (pages 00h, 01h are implemented) 1b=Flat memory (only page 00h implemented)	RO RQD
	6-4	Reserved		
	3-2	TWI Maximum speed	Indicates maximum two-wire serial speed supported by module 00b=Module supports up to 400 kHz 01b=Module supports up to 1 MHz 10b=Reserved 11b=Reserved	RO RQD
	1-0	Reserved		
3	7-4	Reserved		
	3-1	Module state	Current state of Module (see Table 7-3)	RO RQD
	0	Interrupt	Digital state of Interrupt output signal 0b=Interrupt asserted 1b=Interrupt not asserted (default)	

Table 7-3 Module State Encodings

Code	Module state
000b	Reserved
001b	ModuleLowPwr state
010b	ModulePwrUp state
011b	ModuleReady state (reported by flat memory modules)
100b	ModulePwrDn state
101b	Fault state
110b	Reserved
111b	Reserved

7.2.2 Data Path State Indicator

The following fields identify the Data Path State associated with each host lane in the module. Data Path States apply to the host and media interfaces, but are reported by host lane. For data paths with multiple lanes, all lanes shall report the same state. An indication of DataPathDeactivated means no data path is initialized on that lane. Table 7-5 defines the valid Data Path State encodings.

Table 7-4 Data Path State Indicator, per lane (Lower Page) (see Table 7-5

Byte	Bit	Name	Description	Type
4	7-4	Data Path State host lane 2	Data path state encoding, as observed on host lane 2	RO
	3-0	Data Path State host lane 1	Data path state encoding, as observed on host lane 1	RQD

Table 7-5 Data Path State Indicator Encodings

Encoding	State
0h	Reserved
1h	DataPathDeactivated State
2h	DataPathInit State
3h	DataPathDeinit State
4h	DataPathActivated State
5h	DataPathTxTurnOn State
6h	DataPathTxTurnOff State
7h	DataPathInitialized State
8h-Fh	Reserved

7.2.3 Lane-Specific Flags

This section of the memory map contains lane-specific flags. These flags provide a mechanism for reporting lane-specific status changes, faults, operating failures and alarms and warnings for monitored attributes. Each lane-specific flag shall have an associated flag mask. Monitored attributes with associated alarm and/or warning thresholds shall implement associated alarm and warning flags and flag masks. For normal operation and default state, the bits in this field have the value of 0b. Once asserted, the bits remain set (latched) until cleared by a read operation that includes the affected bit or reset by the Reset signal. Note that a read of the flag summary shall not clear the underlying flag condition. If the corresponding mask bit is not set (seeTable 7-15), Interrupt is also asserted at the onset of the condition and remains asserted until all asserted flags (both module-level and lane-specific) have been cleared by a host read. After being read and cleared, the bit shall be set again if the condition persists; this will cause Interrupt to be asserted again unless masked. The lane-specific flags are defined in Table 7-6 and Table 7-7.

A condition, for example, assertion of the TxFault flag, leading to entering the Fault state will assert the TxFault signal. The Txfault signal will remain asserted as long the module is in the Fault state (See 6.3.1.11).

Table 7-6 Lane-Specific State Changed Flags (Lower Page)

Byte	Bit	Name	Description	Type
5	7	L-Lane2 Datapath Operational	Status bit indicating module lane 2 datapath TX/RX including equalizers are set and ready. After one of the stage set registers move into the active set or after a configuration change/speed change affecting the datapath. 0b=Not ready 1b = Ready Default value = 0	RO/COR RQD
	6	L-Lane1 Datapath Operational	Status bit indicating module lane 1 datapath TX/RX including equalizers are set and ready. After one of the stage set registers move into the active set or after a configuration change/speed change affecting the datapath. 0b=Not ready 1b = Ready Default value = 0	
	5	L-Tx Adaptive Input eq Failure flag, host lane 2	Latched Tx Adaptive Input Equalization Failure flag for host lane 2	
	4	L-Tx Adaptive Input eq Failure flag, host lane 1	Latched Tx Adaptive Input Equalization Failure flag for host lane 1	
	3	L-Tx Fault flag, media lane 2	Latched Tx Fault flag for media lane 2	
	2	L-Tx Fault flag, media lane 1	Latched Tx Fault flag for media lane 1	
	1	L-Data Path State Changed flag, host lane 2	Latched Data Path State Changed flag for host lane 2	
	0	L-Data Path State Changed flag, host lane 1	Latched Data Path State Changed flag for host lane 1	

Table 7-7 Lane-Specific Tx Flags (Lower Page)

Byte	Bit	Name	Description	Type
6	7	L-Rx2 CDR LOL	Latched Rx CDR LOL flag, media lane 2. Clear on Read	RO Opt.
	6	L-Rx1 CDR LOL	Latched Rx CDR LOL flag, media lane 1. Clear on Read	
	5	L-Rx2 LOS	Latched Rx LOS flag, media lane 2. Clear on Read	
	4	L-Rx1 LOS	Latched Rx LOS flag, media lane 1. Clear on Read	
	3	L-Tx2 CDR LOL flag	Latched Tx CDR LOL flag, lane 2. Clear on Read	
	2	L-Tx1 CDR LOL flag	Latched Tx CDR LOL flag, lane 1. Clear on Read	
	1	L-Tx2 LOS flag	Latched Tx LOS flag, lane 2	
	0	L-Tx1 LOS flag	Latched Tx LOS flag, lane 1	
7	7	L-Rx2 Power Low warning	Rx input power Low warning, media lane 2. Clear on Read	RO Opt.
	6	L-Rx1 Power Low warning	Rx input power Low warning, media lane 1. Clear on Read	
	5	L-Rx2 Power High warning	Rx input power High warning, media lane 2. Clear on Read	
	4	L-Rx1 Power High warning	Rx input power High warning, media lane 1. Clear on Read	
	3	L-Rx2 Power Low alarm	Rx input power Low alarm, media lane 2. Clear on Read	
	2	L-Rx1 Power Low alarm	Rx input power Low alarm, media lane 1. Clear on Read	
	1	L-Rx2 Power High alarm	Rx input power High alarm, media lane 2. Clear on Read	
	0	L-Rx1 Power High alarm	Rx input power High alarm, media lane 1. Clear on Read	
8	7	L-Tx2 Power Low warning	Tx output power Low warning, media lane 2. Clear on Read	RO Opt.
	6	L-Tx1 Power Low warning	Tx output power Low warning, media lane 1. Clear on Read	
	5	L-Tx2 Power High warning	Tx output power High warning, media lane 2. Clear on Read	
	4	L-Tx1 Power High warning	Tx output power High warning, media lane 1. Clear on Read	
	3	L-Tx2 Power Low alarm	Tx output power Low alarm, media lane 2. Clear on Read	
	2	L-Tx1 Power Low alarm	Tx output power Low alarm, media lane 1. Clear on Read	
	1	L-Tx2 Power High alarm	Tx output power High Alarm, media lane 2. Clear on Read	
	0	L-Tx1 Power High alarm	Tx output power High Alarm, media lane 1. Clear on Read	

Byte	Bit	Name	Description	Type
9	7	L-Tx2 Bias Low warning	Tx Bias Low warning, media lane 2. Clear on Read	RO Opt.
	6	L-Tx1 Bias Low warning	Tx Bias Low warning, media lane 1. Clear on Read	
	5	L-Tx2 Bias High warning	Tx Bias High warning, media lane 2. Clear on Read	
	4	L-Tx1 Bias High warning	Tx Bias High warning, media lane 1. Clear on Read	
	3	L-Tx2 Bias Low alarm	Tx Bias Low alarm, media lane 2. Clear on Read	
	2	L-Tx1 Bias Low alarm	Tx Bias Low alarm, media lane 1. Clear on Read	
	1	L-Tx2 Bias High Alarm	Tx Bias High Alarm, media lane 2. Clear on Read	
	0	L-Tx1 Bias High Alarm	Tx Bias High Alarm, media lane 1. Clear on Read	

7.2.4 Module-Level Flags

This section of the memory map contains module-level flags. These flags provide a mechanism for reporting module-level status changes, faults, errors, operating failures and alarms and warnings for monitored attributes. Each module-level flag shall have an associated flag mask. Monitored attributes with associated alarm and/or warning thresholds shall implemented associated alarm and warning flags and flag masks. For normal operation and default state, the bits in this field have the value of 0b. Once asserted, the bits remain set (latched) until cleared by a read operation that includes the affected bit or reset by the Reset signal. Note that a read of the flag summary shall not clear the underlying flag condition. If the corresponding mask bit is not set (see Table 7-16), Interrupt is also asserted at the onset of the condition and remains asserted until all asserted flags (both module-level and lane-specific) have been cleared by a host read. After being read and cleared, the bit shall be set again if the condition persists; this will cause Interrupt to be asserted again unless masked. The module-level flags are defined in Table 7-8. Byte 13 is provided for Custom Module Level Flags. Some module-level flags are disallowed in certain Module States, refer to section 6.3.3 for details.

A module safety and/or laser eye safty condition module shall enter the Fault state and the TxFault signal is asserted. The Txfault signal will remain asserted as long the module is in the Fault state (See 6.3.1.11).

Table 7-8 Module Flags (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
10	7	L-CDB block 2 complete	Latched flag to indicate completion of the CDB command for CDB block 2. Clear on Read (See Page 01h, Byte 163 bit 7)	RO Opt.
	6	L-CDB block 1 complete	Latched flag to indicate completion of the CDB command for CDB block 1. Clear on Read (See Page 01h, Byte 163 bit 6)	RO Opt.
	5-3	Reserved		RQD
	2	Data Path Firmware Error	Some modules may contain an auxiliary device for processing the transmitted and received signals (e.g. a DSP). The Data Path Firmware Error flag becomes set when an integrity check of the firmware for this auxiliary device finds an error.	RO Opt.
	1	Module Firmware Error	The Module Firmware Error flag becomes set when an integrity check of the module firmware finds an error. There are several possible causes of the error such as program memory becoming corrupted and incomplete firmware loading.	RO Opt.
	0	L-Module state changed flag	Latched Indication of change of Module state (see Table 7-4) Clear on Read	RO RQD
11	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag. Clear on Read	RO Opt.
	6	L-Vcc3.3v High Warning	Latched high 3.3 volts supply voltage warning flag. Clear on Read	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag. Clear on Read	
	4	L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm flag. Clear on Read	
	3	L-Temp Low Warning	Latched low temperature warning flag. Clear on Read	
	2	L-Temp High Warning	Latched high temperature warning flag. Clear on Read	
	1	L-Temp Low Alarm	Latched low temperature alarm flag. Clear on Read	
	0	L-Temp High Alarm	Latched high temperature alarm flag. Clear on Read	
12	7	Reserved		RO Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	L-Aux 1 Low Warning	Latched low warning for Aux 1 monitor. Clear on Read	
	2	L-Aux 1 High Warning	Latched high warning for Aux 1 monitor. Clear on Read	
	1	L-Aux 1 Low Alarm	Latched low alarm for Aux 1 monitor. Clear on Read	
	0	L-Aux 1 High Alarm	Latched high alarm for Aux 1 monitor. Clear on Read	
13	7	L-Vendor Defined Low Warning	Latched low warning for Vendor Defined Monitor. Clear on Read	RO Opt.
	6	L-Vendor Defined High Warning	Latched high warning for Vendor Defined Monitor. Clear on Read	
	5	L-Vendor Defined Low Alarm	Latched low alarm for Vendor Defined Monitor. Clear on Read	
	4	L-Vendor Defined High Alarm	Latched high alarm for Vendor Defined Monitor. Clear on Read	
	3	Reserved		
	2	Reserved		
	1	Reserved		
	0	Reserved		

7.2.5 Module-Level Monitors

Real time monitoring for the module includes temperature, supply voltage, auxiliary and vendor defined monitors as shown in Table 7-9.

The data format may facilitate greater resolution and range than required. Measurement accuracy is defined by the interoperability standard or module product specification.

Table 7-9 Module Monitors (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
14	7-0	Module Monitor 1: Temperature MSB	Internally measured temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Temp can be below 0.	RO Opt.
15	7-0	Module Monitor 1: Temperature LSB		
16	7-0	Module Monitor 2: Supply 3.3-volt MSB	Internally measured 3.3 volt input supply voltage: in 100 µV increments	RO Opt.
17	7-0	Module Monitor 2: Supply 3.3-volt LSB		
18	7-0	Module Monitor 3: Aux 1 MSB	TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 100%/32767 increments of maximum TEC current i.e. the larger of the magnitudes of the heating or cooling currents +32767 is 100% of the max current magnitude when heating -32767 is 100% of the max current when cooling Laser temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Temp can be below 0.	RO Opt.
19	7-0	Module Monitor 3: Aux 1 LSB		
20	7-0	Custom Monitor: Custom MSB	Custom monitor	RO Opt.
21	7-0	Custom Monitor: Custom LSB		

7.2.6 Module Media Lane to Module Media Wavelength and Fiber Mapping

Table 7-10 contains the advertising fields to define the mapping of module media lanes to module media wavelengths and physical fibers for muxed or WDM implementations. For WDM applications the shortest wavelength is always designated media wavelength 1 and starting from shortest wavelength through the longest all others are listed consecutively. The fiber numbers and names used in Table 7-10 are as defined in the appropriate hardware specification. See the relevant hardware specification and Table 7-24, Table 7-34, and Table 7-35 within for mapping constraints. Any mapping advertised in Table 7-10 that violates any of these constraints will not be a valid mapping.

Table 7-10 Module Media Lane to Module Media Wavelength and Fiber mapping (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
22	7-4	Module Tx media lane 1 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 1 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101-1111= Reserved	
23	7-4	Module Tx media lane 2 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 2 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101-1111= Reserved	
24	7-4	Module Rx media lane 1 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 1 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101-1111= Reserved	
25	7-4	Module Rx media lane 2 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 2 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101-1111= Reserved	

7.2.7 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Note: Lane-specific controls are located in Upper page 01h (see Table 7-53*).*

Table 7-11 Module Global and Squelch Mode Controls (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
26	7	IntL/TxFaultDD Control	IntL/TxFaultDD output signal control for pad 22, also controls which lanes reports a fault condition on pad 2 0b = IntL (& pad 2 reports Tx faults conditions for both Tx lanes) 1b = TxFaultDD (& pad 2 reports Tx faults conditions for only lane 0) Default value = 0	RW RQD
	6	LowPwr	A parameter used to control the module power mode. See section 6.3.1.1 for usage Default value = 1	RW RQD
	5	Squelch mode control	0b=Tx Squelch reduces OMA 1b=Tx Squelch reduces Pave (See Table 7-42 for capability advertising)	RW Opt.
	4	ForceLowPwr	1b=Forces module into low power mode – see section 6.3.1.3	RW RQD
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the ResetL signal for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b=Not in reset 1b=Software reset	RW RQD
	2-0	Custom		
27-28	All	Reserved		
29-30	All	Custom	Custom Global controls	

7.2.8 Module-Level Flag Masks

The host may control which flags may cause a hardware Interrupt being asserted to the host by setting masking bits in Table 7-12.

For each flag bit there is a corresponding masking bit. Masking bits are set when their value is or becomes 1. Masking bits are cleared when their value is or becomes 0.

The module behaves as follows: a set masking bit prevents assertion of the hardware interrupt signal by the corresponding latched flag bit. A cleared masking bit, when the corresponding flag bit is the only reason for the hardware Interrupt signal being asserted, de-asserts the hardware Interrupt signal. Masking bits are volatile: at exit from MgmtInit (see section 6.3.1.6), all mask bits shall be clear.

The host may use the masking bits to prevent continued hardware Interrupt assertion from stable conditions, i.e. from asserted flag bits, which would otherwise continually reassert the hardware Interrupt signal.

7.2.9 CDB Status

The CDB Status fields provide the status of the most recently triggered CDB command. For modules that support CDB background operation (see Table 7-46), the host may read the CDB Status field while a CDB command is executing to obtain its current status. For modules that do not support CDB background operation, the host may read the CDB status field after the command has completed, determined through NACK polling.

Table 7-12 CDB Status fields (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
37	7-0	CDB Block 1 status	Status of the most recently triggered CDB command in CDB Block 1	RO Opt.
38	7-0	CDB Block 2 status	Status of the most recently triggered CDB command in CDB Block 2	RO Opt.

Each CDB Status field has the following format:

Table 7-13 Bit definitions within CDB Status fields (Lower Page, active modules only)

Bits	Name	Description
7	STS_BUSY	One-bit value indicating the availability of the CDB interface 0b=Module idle, host can write 1b=Module busy, host needs to wait
6	STS_FAIL	0b=Last triggered CDB command completed successfully 1b=Last triggered CDB command failed, see Last Command Result field for details
5-0	Last command result	**Note: The following fields depend on the values of bits 6,7.** **STS_BUSY=1, STS_FAIL=X (IN PROGRESS)** 00h=Reserved 01h=Command is captured but not processed 02h=Command checking is in progress 03h=Command execution is in progress 04h-2Fh=Reserved 30h-3Fh=Custom **STS BUSY=0, STS_FAIL=0 (SUCCESS)** 00h=Reserved 01h=Command completed successfully without specific message 02h=Reserved 03h=Previous CMD was ABORTED by CMD Abort 04h-1Fh=Reserved 20h-2Fh=Reserved 30h-3Fh=Custom **STS_BUSY=0, STS_FAIL=1 (FAILED)** 00h=Reserved 01h=CMD Code unknown 02h=Parameter range error or not supported 03h=Previous CMD was not ABORTED by CMD Abort 04h=Command checking time out 05h=CdbCheckCode Error 06h=Password error 07h-0Fh=Reserved for STS command checking error 10h-1Fh=Reserved 20h-2Fh=For individual STS command or task error 30h-3Fh=Custom

Each CDB status field is located in lower memory so that page changes are not needed to read it. Both of these fields are initialized to 0 before exiting MgmtInit (see section 6.3.1.6).

The module updates the STS_BUSY bit to 1b when a CDB command is triggered on the respective block. When a CDB command completes, the module sets the STS_BUSY bit to 0b and sets the STS_FAIL and Last Command Result fields according to the result of the completed command. All subfields within a CDB Status byte remain unchanged until the next CDB command is triggered for the respective block.

7.2.10 Module Active Firmware Version

Bytes in Table 7-14 allows a module to return the active (current running) firmware major and minor revision. Flat memory modules that has firmware running may report it's firmware version in these bytes.

The encoding or major and minor revision are:

- Major Revision = 0 and Minor Revision = 0 indicates that a module does not have any firmware.
- Major Revision = FFh and Minor Revision = FFh indicates that a module active firmware image is bad.
- All other Major and Minor Revision combinations are used to indicate the active firmware version.

Table 7-14 Module Active Firmware Version

Byte	Bits	Name	Description	Type
39	7-0	Active Module firmware major revision	Numeric representation of Active module firmware major revision	RO Opt.
40	7-0	Active Module firmware minor revision	Numeric representation of Active module firmware minor revision	RO Opt.

A module having an active firmware version may or may not have an inactive version. A module supporting paged memory may also advertise an inactive image in the bytes described in section 7.4.1 which has the same encodings. Content of the firmware major and minor revisions reported back are vendor dependent. Modules that supports a proprietary vendor dependent firmware upgrade methodology (not CDB as described later) may still report firmware active or inactive versions in these bytes.

7.2.11 Lane-Specific Flag Masks

The host may control which flags result in a hardware interrupt by setting masking bits in Table 7-15. For example, the mask bits may be used to prevent an interrupt request from remaining active while the host performs actions to acknowledge and handle the interrupt condition. A mask bit is allocated for each flag bit.

A value of 1 in a masking bit prevents the assertion of the hardware interrupt signal, if one exists, by the corresponding latched flag bit. Masking bits are volatile: at exit from MgmtInit (see section 6.3.1.6), all mask bits shall be clear.

Table 7-15 Lane-Specific Flag Masks (Lower Page)

Byte	Bits	Name	Description	Type
53	7	L-Lane2 DatapathOp flag mask	Masking bit indicating module lane 2 datapath TX/RX including equalizers are ready	RW RQD
	6	L-Lane1 DatapathOp flag mask	Masking bit indicating module lane 1 datapath TX/RX including equalizers are ready	
	5	M-Tx2 Adaptive Eq Failure flag mask	Masking bit for Tx Adaptive Input Eq Failure lane 2	
	4	M-Tx1 Adaptive Eq Failure flag mask	Masking bit for Tx Adaptive Input Eq Failure lane 1	
	3	M-Tx2 Fault flag mask	Masking bit for Tx Fault flag, media lane 2	
	2	M-Tx1 Fault flag mask	Masking bit for Tx Fault flag, media lane 1	
	1	M-Data Path State Changed flag mask, host lane 2	Masking bit for Data Path State Changed flag, host lane 2	
	0	M-Data Path State Changed flag mask, host lane 1	Masking bit for Data Path State Changed flag, host lane 1	
54	7	M-Rx2 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 2	RW Opt.
	6	M-Rx1 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 1	
	5	M-Rx2 LOS flag mask	Masking bit for Rx LOS flag, media lane 2	
	4	M-Rx1 LOS flag mask	Masking bit for Rx LOS flag, media lane 1	
	3	M-Tx2 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 2	
	2	M-Tx1 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 1	
	1	M-Tx2 LOS flag mask	Masking bit for Tx LOS flag, lane 2	
	0	M-Tx1 LOS flag mask	Masking bit for Tx LOS flag, lane 1	
55	7	M-Rx2 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 2	RW Opt.
	6	M-Rx1 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 1	
	5	M-Rx2 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 2	
	4	M-Rx1 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 1	
	3	M-Rx2 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 2	
	2	M-Rx1 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 1	
	1	M-Rx2 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 2	
	0	M-Rx1 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 1	
56	7	M-Tx2 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 2	RW Opt.
	6	M-Tx1 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 1	
	5	M-Tx2 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 2	
	4	M-Tx1 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 1	
	3	M-Tx2 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 2	
	2	M-Tx1 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 1	
	1	M-Tx2 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 2	
	0	M-Tx1 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 1	
57	7	M-Tx2 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 2	RW Opt.
	6	M-Tx1 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 1	
	5	M-Tx2 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 2	
	4	M-Tx1 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 1	
	3	M-Tx2 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 2	
	2	M-Tx1 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 1	
	1	M-Tx2 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 2	
	0	M-Tx1 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 1	

Table 7-16 Module Level Flag Masks (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
58	7	M-CDB Block 2 complete	Masking bit for CDB Block 2 Complete flag	RW Opt.
	6	M-CDB Block 1 complete	Masking bit for CDB Block 1 Complete flag	RW Opt.
	5-3	Reserved		RO
	2	M-Data Path Firmware Error	Masking bit for Data Path Firmware Error flag	RW Opt.
	1	M-Module Firmware Error	Masking bit for Module Firmware Error flag	RW Opt.
	0	M-Module State changed flag mask	Masking bit for Module State Changed flag	RW RQD
59	7	M-Vcc3.3 Low Warning flag mask	Masking bit for Vcc3.3 monitor low warning flag	RW Opt.
	6	M-Vcc3.3 High Warning flag mask	Masking bit for Vcc3.3 monitor high warning flag	
	5	M-Vcc3.3 Low Alarm flag mask	Masking bit for Vcc3.3 monitor low alarm flag	
	4	M-Vcc3.3 High Alarm flag mask	Masking bit for Vcc3.3 monitor high alarm flag	
	3	M-Temp Low Warning flag mask	Masking bit for temperature monitor low warning flag	
	2	M-Temp High Warning flag mask	Masking bit for temperature monitor high warning flag	
	1	M-Temp Low Alarm flag mask	Masking bit for temperature monitor low alarm flag	
	0	M-Temp High Alarm flag mask	Masking bit for temperature monitor high alarm flag	
60	7	Reserved		RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	M-Aux 1 Low Warning flag mask	Masking bit for Aux 1 monitor low warning flag	
	2	M-Aux 1 High Warning flag mask	Masking bit for Aux 1 monitor high warning flag	
	1	M-Aux 1 Low Alarm flag mask	Masking bit for Aux 1 monitor low alarm flag	
	0	M-Aux 1 High Alarm flag mask	Masking bit for Aux 1 monitor high alarm flag	
61	7	M-Vendor Defined Low Warning flag mask	Masking bit for Vendor defined low warning flag	RW Opt.
	6	M-Vendor Defined High Warning flag mask	Masking bit for Vendor defined high warning flag	
	5	M-Vendor Defined Low Alarm flag mask	Masking bit for Vendor defined low alarm flag	
	4	M-Vendor Defined High Alarm flag mask	Masking bit for Vendor defined high alarm flag	
	3	Reserved		
	2	Reserved		
	1	Reserved		
	0	Reserved		

7.2.12 Lane-Specific Monitors

Real time lane monitoring may be performed for each transmit and receive lane and includes Tx output optical power, Rx input optical power, and Tx bias current. Alarm threshold values and warning threshold values have the same numerical value representation as the associated monitor values for which they specify threshold values.

Measured Tx bias current is represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 to 65535) with LSB equal to 2 uA times the multiplier from page 01h byte 160. For a multiplier of 1, this yields a total measurement range of 0 to 131 mA. Accuracy is Vendor Specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.

Measured Rx input optical power is in mW and can represent either average received power or OMA depending the Rx Optical Power Measurement type in Table 7-41. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is Vendor Specific.

Measured Tx optical power is the average power represented in mW. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage.

Table 7-17 Media Lane-Specific Monitors (Lower Page)

Byte	Bit	Name	Description	Type
62	7-0	Tx1 Power MSB	Internally measured Tx output optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	RO Opt.
63	7-0	Tx1 Power LSB		
64	7-0	Tx2 Power MSB		
65	7-0	Tx2 Power LSB		
66	7-0	Tx1 Bias MSB	Internally measured Tx bias current monitor: unsigned integer in 2 uA increments, times the multiplier from Table 7-44.	RO Opt.
67	7-0	Tx1 Bias LSB		
68	7-0	Tx2 Bias MSB		
69	7-0	Tx2 Bias LSB		
70	7-0	Rx1 Power MSB	Internally measured Rx input optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	RO Opt.
71	7-0	Rx1 Power LSB		
72	7-0	Rx2 Power MSB		
73	7-0	Rx2 Power LSB		

7.2.13 Configuration Error Codes

The configuration requested by the host in either Staged Set may not be supported by the module for a variety of reasons. The Configuration Error Code registers are defined to provide feedback to the host software for cases where an invalid configuration was requested.

A code is provided for each lane (see Table 7-18). In cases where the feedback is data path-wide, the module shall populate all lanes in the data path with the same code. The applicable Configuration Error Code registers shall be populated by the module when the host sets one or more bits in Apply_DataPathInit or Apply_Immediate, before the requested configuration is copied into the Active Set. If the configuration was determined to be invalid by the module, the configuration shall not be copied into the Active Set. Any configuration error code greater than or equal to 2 indicates a rejected configuration.

Table 7-18 Configuration Error Code registers (Lower Page)

Byte	Bit	Name	Description	Type
74	7-4	Lane 2 Config Error Code	Configuration Error Code for lane 2	RO
	3-0	Lane 1 Config Error Code	Configuration Error Code for lane 1	Opt.

Table 7-19 Configuration Error Codes (Lower Page)

Encoding	Name	Description
0h	No status	No status information available or config in process
1h	Config accepted	Configuration accepted and successfully applied
2h	Config rejected unknown	Configuration rejected for unknown reason
3h	Config rejected invalid code	Configuration rejected due to invalid ApSel Code request
4h	Config rejected invalid combo	Configuration rejected due to ApSel Code requested on invalid lane combination
5h	Config rejected invalid SI	Configuration rejected due to Invalid SI control set request
6h	Config rejected in use	Configuration rejected due to portion of lane group currently in use for a different Application (in order to switch to an Application with a different lane width, all lanes in the target Data Path must be in DataPathDeactivated)
7h	Config rejected incomplete lane info	DataPathInit requested with incomplete lane information
8h-Ch	Reserved	
Dh-Fh	Custom	Configuration rejected for custom reason

7.2.14 Active Control Set

The Active Control Set is required for all modules. Refer to section 6.2.3 for background on Control Set methodology.

Before exiting the MgmtInit state, the Active Control Set may be populated with a default Application Code and signal integrity settings. The host may update the Active Control Set by using the Apply_DataPathInit or Apply_Immediate control fields in either Staged Set 0 or Staged Set 1. See section 7.4.18 for a description of Control Set usage.

7.2.14.1 Application Select Fields

The following fields allow the host to infer the current baud rate, modulation format, and data path width for each lane in the module.

The ApSel Code shall be one of the module-advertised ApSel Codes from Table 7-24 or a value of 0000b to indicate that the applicable lane is not part of any data path. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane number would be coded 100b. Explicit Control (bit 0 in bytes 206-213) indicates the host has specified signal integrity settings rather than using the Application-defined settings.

Table 7-20 Indicators for Active Control Set, Application Selected (Lower Page)

Byte	Bits	Name	Description	Type
75	7-4	Active Set Lane 1 ApSel code	ApSel Code from Table 7-24 lane 1	RO RQD
	3-1	Active Set Lane 1 Data Path ID	First lane in the data path containing lane 1 000b=Lane 1	
	0	Active Set Lane 1 Explicit Control	0b=Lane 1 settings are Application-defined 1b=Lane 1 settings are host-specified	
76	7-4	Active Set Lane 2 ApSel code	ApSel Code from Table 7-24 lane 2	RO RQD
	3-1	Active Set Lane 2 Data Path ID	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2	
	0	Active Set Lane 2 Explicit Control	0b=Lane 2 settings are Application-defined 1b=Lane 2 settings are host-specified	

7.2.14.2 Tx and Rx Signal Integrity Fields

The following fields allow the host to view the signal integrity settings for a lane. If the Explicit Control bit for a lane is set, the module is using the host-defined settings from Table 7-54 and Table 7-58. If the Explicit Control bit for a lane is clear, the module is using Application-defined default signal integrity settings. See section 6.2.4 for definitions of valid signal integrity control settings.

Table 7-21 Indicators for Active Control Set, Tx Controls (Lower Page)

Byte	Bits	Name	Description	Type
77	7-6	Reserved		
	5	Active Set Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 217 Page 11h	RO Opt.
	4	Active Set Tx1 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 217 Page 11h	
	3-2	Active Set Tx2 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See Table 7-54 and Table 7-58	
	1-0	Active Set Tx1 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See Table 7-54 and Table 7-58	
78	7-4	Active Set Tx2 Input Eq control	Manual fixed Tx input eq control[1]	RO Opt.
	3-0	Active Set Tx1 Input Eq control	Manual fixed Tx input eq control[1]	
79	7-6	Reserved		
	5	Active Set Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	RO Opt.
	4	Active Set Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3-2	Reserved		
	1	Active Set Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	RO Opt.
	0	Active Set Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Note 1: See Table 6-4

Table 7-22 Indicators for Active Control Set, Rx Controls (Lower Page)

Byte	Bits	Name	Description	Type
80	7-4	Active Set Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RO Opt.
	3-0	Active Set Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
81	7-4	Active Set Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RO Opt.
	3-0	Active Set Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
82	7-4	Active Set Rx2 Output Amplitude control	Rx output amplitude encoding[2]	RO Opt.
	3-0	Active Set Rx1 Output Amplitude control	Rx output amplitude encoding[2]	

Note 1: See Table 6-5
Note 2: See Table 6-6

7.2.15 Application Advertising

Table 7-24 provides space for the first four bytes of up to eight Application descriptors. The remaining fifth byte (Media Lane Assignment Options) of each Application descriptor is stored in a separate Table 7-49.

All modules shall advertise at least one Application. The Host Electrical Interface ID field of the first unused entry in Table 7-24 shall be set to a value of FFh to indicate the end of the list of valid Application descriptors.

Note: Application descriptors are used by the module to advertise supported Applications. See section 6.2.1.1 *for more information about Application advertising* .

Host Electrical Interface IDs and Module Media Interface IDs are specified in Table 7-23.

The Module Type Encoding field (Byte 85) indicates which particular Media Interface Type table applies to the module. Valid Module Type Encoding values are specified in Table 7-23.

The host lane count and media lane count fields specify the number of lanes either explicitly (nonzero value) or by implicit reference, via the interface ID, to the relevant interface specification (zero value).

The host lane assignment options specify which lane groups can be used for a Data Path carrying the advertised application. Bits 0-7 form a bit map corresponding to Host Lanes 1-8. A bit value of 1 indicates that the lane group of the advertised Application can begin on the corresponding host lane. See section 6.2.1.1 for a more detailed description.

Table 7-23 Byte 85 Module Media Type Encodings (Type RO RQD)

Code	Module Media Type	Associated Interface ID Table
00h	Undefined	
01h	Optical Interfaces: MMF	SFF-8024 IDs for 850 nm Multi-Mode Media Interfaces
02h	Optical Interfaces: SMF	SFF-8024 IDs for Single-Mode Media Interfaces
03h	Passive Cu	SFF-8024 IDs for Passive Copper Cable Media Interfaces
04h	Active Cables	SFF-8024 IDs for Active Copper Cable Media Interfaces
05h	BASE-T	SFF-8024 IDs for BASE-T Media Interfaces
06h-3Fh	Reserved	
40h-8Fh	Custom	
90h-FFh	Reserved	

Table 7-24 Application Advertising Fields (Lower page)

Byte	Bits	ApSel Code	Name	Description	Type
86	7-0	0001b	Host Electrical Interface ID	ID from SFF-8024 IDs for Host Electrical Interfaces	RO RQD
87	7-0		Module Media Interface ID	ID from table selected by Byte 85 (see Table 7-23)	
88	7-4		Host Lane Count	0000b=lane count defined by interface ID 0001b=1 lane, 0010b=2 lanes 0011b-1111b=reserved	
	3-0		Media Lane Count		
89	7-0		Host Lane Assignment Options (See Table 7-49 for Media Lane Assignment Options)	Bits 0-1 form a bit map and correspond to Host Lanes 1-2. A bit value 1 indicates that the Application may begin on the corresponding host lane. Refer to section 6.2.1.1 for details.	
90	7-0	0010b	Host Electrical Interface ID	See ApSel Code 0001b Coded FFh if first unused ApSel code	RO Opt.
91	7-0		Module Media Interface ID	See ApSel Code 0001b	
92	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
93	7-0		Host Lane Assign Options	See ApSel Code 0001b	
94	7-0	0011b	Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
95	7-0		Module Media Interface ID	See ApSel Code 0001b	
96	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
97	7-0		Host Lane Assign Options	See ApSel Code 0001b	
98	7-0	0100b	Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
99	7-0		Module Media Interface ID	See ApSel Code 0001b	
100	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
101	7-0		Host Lane Assign Options	See ApSel Code 0001b	
102	7-0	0101b	Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
103	7-0		Module Media Interface ID	See ApSel Code 0001b	
104	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
105	7-0		Host Lane Assign Options	See ApSel Code 0001b	
106	7-0	0110b	Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
107	7-0		Module Media Interface ID	See ApSel Code 0001b	
108	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
109	7-0		Host Lane Assign Options	See ApSel Code 0001b	
110	7-0	0111b	Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
111	7-0		Module Media Interface ID	See ApSel Code 0001b	
112	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
113	7-0		Host Lane Assign Options	See ApSel Code 0001b	
114	7-0	1000b	Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
115	7-0		Module Media Interface ID	See ApSel Code 0001b	
116	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
117	7-0		Host Lane Assign Options	See ApSel Code 0001b	

7.2.16 Password Entry and Change

The host system manufacturer password shall fall in the range of 00000000h to 7FFFFFFFh, and all module manufacturer passwords in the range of 80000000h to FFFFFFFFh. The host system manufacturer password shall be initially set to 00001011h in new modules.

The host system manufacturer password may be changed by writing a new password in Bytes 118-121 when the correct current host system manufacturer password has been entered in Bytes 122-125, with the high order bit being ignored and forced to a value of 0 in the new password. The password entry field shall be set to 00000000h on power up and reset.

Table 7-25 Password Change Entry

Byte	Bits	Name	Description	Type
118-121	7-0	Password Change Entry Area		WO Opt.
122-125	7-0	Password Entry Area		WO Opt.

7.2.17 Bank Select Byte

The value written to the Bank Select byte 126 determines which bank is accessed when banking is supported.

The host shall write the bank select and page select registers in one TWI transaction when a bank change is required, even if the page number is not changing.

The module shall not begin processing the new bank select setting until after the page select register is written.

Writing the value of a non-supported bank shall be ignored by the module. The Bank Select byte shall also be ignored if the memory map address being accessed is less than or equal to 127.

Writing the value of a non-supported bank and page combination shall not be accepted by the module. In this case the module shall set the Page Select byte to 0. Since page 00h is less than 10h, the module ignores the invalid bank select byte and returns the contents of page 00h in subsequent memory map read/write operations.

The module shall not begin processing the new bank select setting until the page select register is written. The timing for adjustments to the upper data bank and pages is specified in 7.2.19 and applies to both supported and non-supported values.

7.2.18 Page Select Byte

The value of the Page Select byte 127 determines which page is accessed when a TWI based read or write command accesses byte addresses 128 through 255.

A value of 00h indicates Page 00h is mapped to Bytes 128-255 and a value of 01h indicates that Page 01h if available is mapped to Bytes 128-255. Similarly, values of 02h, 03h, etc., indicate that the page identified by the bank select byte is mapped to Bytes 128-255.

Writing the value of a non-supported page or a non-supported bank and page combination shall not be accepted by the module. In such cases the Page Select byte shall revert to 0 and read/write operations shall be to page 00h.

For a bank change, the host shall write the Bank Select and Page Select registers in the same TWI transaction.

For a bank change, the host shall write the Bank Select and page Select registers in the same TWI transaction. The timing for adjustments to the upper data bank and pages is specified in 7.2.19 and applies to both supported and non-supported values.

7.2.19 Timing of Bank and Page Select

When the bank or page are changed as defined in sections 7.2.17 and 7.2.18 the module shall ensure that access to the new bank and page bytes is available within 500 us of the STOP condition (LOW to HIGH SDA transition with HIGH SCL) of the write transaction that caused the change. The module may further employ clock stretching up to the maximum allowable clock stretch timing pertinent to the respective specification. This increases the time before access to the new bank and page is available beyond 500 μs.

7.3 Upper Memory - Page 00h (Administrative Information)

Upper page 00h contains static read-only module identification information. Upper page 00h shall be implemented for both paged and flat memory implementations and is required for all modules and cable assemblies.

Table 7-26 Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-207	6	Copper Cable Attenuation	
208-209	2	Reserved	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

7.3.1 Identifier

The identifier value specifies the physical device implementation and, by inference, memory map data format. This field should contain the same value as byte 0 in lower memory. These values are maintained in the Transceiver Management section of SFF-8024.

Table 7-27 Identifiers (Page 00h)

Byte	Bits	Name	Description	Type
128	7-0	Identifier	Identifier - Type of Serial Module - See SFF-8024.	RO RQD

7.3.2 Vendor Name (Page 00h, Bytes 129-144, RO, required)

The vendor name is a required 16 character field (bytes 129-144) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. The vendor name may be the original manufacturer of the module or the name of the module reseller. In both cases, the Vendor Name and Vendor OUI (if specified) shall correlate to the same company. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

7.3.3 Vendor Organizationally Unique Identifier (Page 00h, Bytes 145-147, RO, required)

The vendor organizationally unique identifier field (vendor OUI) is a required 3-byte field (bytes 145-147) that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

7.3.4 Vendor Part Number (Page 00h, Bytes 148-163, RO, required)

The vendor part number (vendor PN) is a required 16-byte field (bytes 148-163) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor part number is unspecified.

7.3.5 Vendor Revision Number (Page 00h, Bytes 164-165, RO, required)

The vendor revision number (vendor rev) is a required 2-byte field (bytes 164-165) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

7.3.6 Vendor Serial Number (Page 00h, Bytes 166-181, RO, required)

The vendor serial number (vendor SN) is a required 16-character field (bytes 166-181) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the Product. A value of all zero in the 16-byte field indicates that the vendor serial number is unspecified.

7.3.7 Date Code

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the following format:

Table 7-28 Date Code (Page 00h)

Byte	Bits	Name	Description	Type
182-183	All	Date code year	ASCII code, two low order digits of year (00=2000)	RO RQD
184-185	All	Date code month	ASCII code digits of month (01=Jan through 12=Dec)	RO RQD
186-187	All	Date code day of month	ASCII code day of month (01-31)	RO RQD
188-189	All	Lot code	ASCII code, custom lot code, may be blank	RO Opt.

7.3.8 CLEI Code

The CLEI (Common Language Equipment Identification) code is a 10-byte field (bytes 190-199) that contains the vendor's CLEI code in ASCII characters. The CLEI code is optional. If CLEI code is not implemented a value of ASCII 20h (space) shall be entered.

7.3.9 Module Power Characteristics

The module power characteristics are defined in the two memory locations in Table 7-29. The power class identifier and max power field both specify maximum power consumption over operating conditions and lifetime with all supported settings set to worst case values. See section 6.3.1.3 for details.

Table 7-29 Module Power Class and Max Power (Page 00h)

Byte	Bits	Name	Description	Type
200	7-5	Module Card Power Class[1]	000: Power class 1 001: Power class 2 010: Power class 3 011: Power class 4 110: Power class 7 111: Power class 8 (see byte 201)	RO RQD
	5-6 4-0	Reserved		RO
201	7-0	Max Power	Maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W	RO RQD

Note 1: See hardware specification for Power class values

7.3.10 Cable Assembly Length

The link length field provides the physical interconnect length of cable assemblies, including both passive copper and active optical or electrical cables. Transceivers with separable optical connectors shall populate this field with a 0. The code 11111111b means that the device supports a link length greater than 6300 m.

Table 7-30 Cable Assembly Length (Page 00h)

Byte	Bits	Name	Description	Type
202	7-6	Length multiplier field (Copper or active cable)	Multiplier for value in bits 5-0. 00 = multiplier of 0.1 01 = multiplier of 1 10 = multiplier of 10 11 = multiplier of 100	RO RQD
	5-0	Base Length field (copper of active cable)	Link length base value in meters. To calculate actual link length use multiplier in bits 7-6.	

7.3.11 Media Connector Type

The Connector Type field indicates the connector type for the media side of the module. These values are maintained in the Connector References section of SFF-8024.

Table 7-31- Media Connector Type (Page 00h)

Byte	Bits	Name	Description	Type
203	7-0	Connector Type	Type of connector present in the module. See SFF-8024 for codes.	RO RQD

7.3.12 Copper Cable Attenuation

These Bytes are used to define the cable attenuation for passive copper cables. For transceiver modules bytes 204-209 are reserved.

Table 7-32 Copper Cable Attenuation (Page 00h)

Byte	Bits	Name	Description	Type
204	7-0	5 GHz attenuation	Passive copper cable attenuation at 5 GHz in 1 dB increments	RO Opt.
205	7-0	7 GHz attenuation	Passive copper cable attenuation at 7 GHz in 1 dB increments	RO Opt.
206	7-0	12.9 GHz attenuation	Passive copper cable attenuation at 12.9 GHz in 1 dB increments	RO Opt.
207	7-0	25.8 GHz attenuation	Passive copper cable attenuation at 25.8 GHz in 1 dB increments	RO Opt.
208-209	All	reserved		RO

7.3.13 Cable Assembly Lane Information

Table 7-33 (Byte 210) is applied to all modules to indicate the number of near end media lanes implemented. With optical cable assemblies a media lane may be a fiber or a wavelength. Far end cable lane group fields (Byte 211) are used for cable assemblies to indicate the number of far end lanes implemented and the far end lane configuration. Far end cable lane group fields do not apply to modules with detachable media connectors. No information is given on the type of module on the far end of the cable (i.e. QSFP, SFP etc.), only the number of modules in the far end.

Table 7-33- Media lane interface implementation (Page 00h)

Byte	Bits	Name	Description	Type
	7-2	Reserved		
210	1	Near end implementation lane 2	0b=Lane 2 implemented in near end 1b=Lane 2 not implemented in near end	RO Opt.
	0	Near end implementation lane 1	0b=Lane 1 implemented in near end 1b=Lane 1 not implemented in near end	
211	7-5	Reserved		RO
	4-0	Far End Configuration	See Table 7-34 for config code of discrete far end connectors	RO Opt.

Table 7-34 contains codes for all near end supported combinations of far end modules (lane groups a to h), and maps those far end modules (lane groups) to the connected near end lane number. Unique letters indicate discrete modules. Note that the discrete modules may or may not be the same module type.

Table 7-34 Far end cable lane groups advertising codes (Page 00h)

Far End Cable Lane Groups Advertising Codes				
Config Code		Near End Host Lane Number		
Decimal	Binary	1	2	
0	00000b	Undefined - Use for detachable modules		
1	00001b	a	b	
2	00010b	a	a	
3-31	00011b-11111b	reserved		

7.3.14 Media Interface Technology (required)

Byte 212 is a required byte that defines aspects of the device or cable technology, using the encodings in Table 7-35. An active optical cable may distinguish from a separable module using Byte 203 (see section 7.3.11).

Table 7-35 Media Interface Technology encodings

Code	Description of physical device
00h	850 nm VCSEL
01h	1310 nm VCSEL
02h	1550 nm VCSEL
03h	1310 nm FP
04h	1310 nm DFB
05h	1550 nm DFB
06h	1310 nm EML
07h	1550 nm EML
08h	Others
09h	1490 nm DFB
0Ah	Copper cable unequalized
0Bh	Copper cable passive equalized
0Ch	Copper cable, near and far end limiting active equalizers
0Dh	Copper cable, far end limiting active equalizers
0Eh	Copper cable, near end limiting active equalizers
0Fh	Copper cable, linear active equalizers
10h-FFh	Reserved

7.3.15 Page 00h Checksum Byte 222, RO Required

The checksum is a one byte code that can be used to verify that the read-only static data on Page 00h is valid. The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 128 to byte 221, inclusive.

7.3.16 Custom Info (non-volatile)

Bytes 223-255 are allocated in the non-volatile storage space for information provided by the original manufacturer of the module or the module reseller. This information persists across module reset and power cycle. The contents of this area are not defined by this specification.

7.4 Page 01h (Advertising)

Page 01h contains advertising fields and control fields that are unique to active modules and cable assemblies. The presence of Page 01h is advertised in bit 7 in Page 00h byte 2.

Table 7-36 Page 01h Overview

Byte	Size (bytes)	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Memory Pages and Durations advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	
157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-166	4	CDB support advertising	
167-168	2	Additional Durations advertising	
169-175	7	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
233	1	DataPathDeinit	Data Pathcontrol bits for each lane, controls Data Path State machine
234-239	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
240-245	35	Staged Control Set 0	Fields to configure the selected Application Code and signal integrity settings
246-254	35	Staged Control Set 1	Fields to configure the selected Application Code and signal integrity settings
255	1	Checksum	Checksum of bytes 130-232[1]

Note 1: The firmware version bytes 128-129 are excluded from the checksum to allow module implementers to programmatically generate these fields and avoid requiring a memory map update when firmware is updated.

7.4.1 Module Inactive Firmware and Hardware Revisions

Table 7-37 describes the memory map locations for reporting module's inactive firmware and the module's hardware revisions. The finished module or cable assembly revision number shall be reported in the Vendor Revision Number field described in section 7.3.5.

The module inactive firmware major and minor revisions shall be represented as numeric values. These two values shall not be included in the Page 01h checksum as these byte may change dynamically for modules that supports switching firmware version between multiple images during firmware upgrades. The inactive firmware is the alternate or backup firmware image that may reside on the module. These bytes have the same special encoding as the active firmware major and minor revisions (see section 7.2.10).

The module hardware major and minor revisions shall be represented as numeric values. These two values shall be included in the Page 01h checksum.

Table 7-37 Module Inactive Firmware and Hardware Revisions (Page 01h)

Byte	Bits	Name	Description	Type
128	7-0	Inactive Module firmware major revision	Numeric representation of inactive module firmware major revision	RO RQD
129	7-0	Inactive Module firmware minor revision	Numeric representation of inactive module firmware minor revision	RO RQD
130	7-0	Module hardware major revision	Numeric representation of module hardware major revision	RO RQD
131	7-0	Module hardware minor revision	Numeric representation of module hardware minor revision	RO RQD

7.4.2 Supported Link Length

These bytes define the maximum supported fiber media length for each type of fiber media at the maximum module-supported bit rate for active modules with a separable optical interface. Unsupported media types shall be populated with zeroes. Active optical cables shall populate the fields in this table with zeroes and instead report their actual length using the fields in Table 7-30.

Table 7-38 Supported Fiber Link Length (Page 01h)

Byte	Bits	Name	Description	Type
132	7-6	Length multiplier(SMF)	Link length multiplier for SMF fiber 00 = 0.1 (1 to 6.3 km) 01 = 1 (1 to 63 km) 10, 11 = reserved	RO RQD
	5-0	Base Length (SMF)	Base link length for SMF fiber. Must be multiplied by value in bits 7-6 to calculate actual link length in km.	
133	7-0	Length (OM5)	Link length supported for OM5 fiber, units of 2 m (2 to 510 m)	RO RQD
134	7-0	Length (OM4)	Link length supported for OM4 fiber, units of 2 m (2 to 510 m)	RO RQD
135	7-0	Length (OM3)	Link length supported for EBW 50/125 µm fiber (OM3), units of 2m (2 to 510 m)	RO RQD
136	7-0	Length (OM2)	Link length supported for 50/125 µm fiber (OM2), units of 1m (1 to 255 m)	RO RQD
137	7-0	Reserved		RORQD

The link length supported for SMF fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using single mode fiber. The supported link length is as specified in the SFF 8074i standard. The value is in units of kilometers.

The link length supported for OM5 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) and 2470 MHz*km (953 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM4 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM3 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 2000 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM2 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) 50 micron multi-mode fiber. The value is in units of one meter.

7.4.3 Wavelength (Page 01h, Bytes 138 - 139, RO, RQD)

The wavelength field specifies the nominal transmitter output wavelength at room temperature; this is a 16-bit value with byte 138 as the high order byte and byte 139 as the low order byte. The laser wavelength value is equal to the 16-bit integer value of the wavelength in nm divided by 20 (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected Applications. For accurate representation of controlled wavelength Applications, this value should represent the center of the guaranteed wavelength range.

7.4.4 Wavelength Tolerance (Page 01h, Bytes 140 - 141, RO, RQD)

The wavelength tolerance is the worst case +/- range of the transmitter output wavelength under all normal operating conditions; this is a 16-bit value with byte 140 as the high order byte and byte 141 as the low order byte. The laser wavelength tolerance is equal to the 16-bit integer value in nm divided by 200 (units of 0.005nm). Thus, the following two examples:

Example 1:

10GBASE-LR Wavelength Range = 1260 to 1355 nm
Nominal Wavelength in bytes 138 - 139 = 1307.5 nm.
Represented as INT (1307.5 nm * 20) = 26150 = 6626h
Wavelength Tolerance in bytes 140 - 141 = 47.5nm.
Represented as INT (47.5 nm * 200) = 9500 = 251Ch.

Example 2:

ITU-T Grid Wavelength = 1534.25 nm with 0.236 nm Tolerance
Nominal Wavelength in bytes 138 - 139 = 1534.25 nm.
Represented as INT (1534.25 nm * 20) = 30685 = 77DDh
Wavelength Tolerance in bytes 140 - 141 = 0.236 nm.
Represented as INT (0.236 nm * 200) = 47 = 002Fh.

7.4.5 Implemented Memory Pages and Durations Advertising

The fields in Table 7-39 advertise module implementation of optional management interface features.

Table 7-39 Implemented Management Interface Features Advertising (Page 01h)

Byte	Bit	Name	Description	Type
142	7-6	Reserved		
	5	Diagnostic pages implemented	Bank page 13h-14h implemented for diagnostic features	RO RQD
	4-3	reserved		
	2	Page 03h implemented	Indicates User page 03h implemented	
	1-0	Implemented Banks[1]	Indicates bank pages implemented for pages 10h-1Fh 00b=bank 0 implemented if a page in that bank is advertised otherwise no bank is implemented 01b=banks 0 and 1 implemented 10b=banks 0. 1. 2, 3 implemented 11b=reserved	
143	7-0	Reserved		
144	7-4	DataPathDeinit_MaxDuration	Encoded maximum duration of the DataPathDeinit state (see Table 7-40)	RO RQD
	3-0	DataPathInit_MaxDuration	Encoded maximum duration of the DataPathInit state (see Table 7-40)	

Note 1: For module response to host attempts to write an invalid bank page combination see sections 7.2.17 and 7.2.18.

The DataPathInit_MaxDuration and DataPathDeinit_MaxDuration fields are defined so host implementers can determine when something has gone wrong in the module during these states, for example a module firmware hang up. These values should be selected to represent the worst-case durations of these two states, across all advertised Applications and combinations of data paths. See sections 6.3.2.3 and 6.3.2.5 for details of the DataPathInit and DataPathDeinit states, respectively.

Table 7-40 State Duration Encoding (Page 01h)

Encoding	Maximum State Duration
0000b	Maximum state duration is less than 1 ms
0001b	1 ms <= maximum state duration < 5 ms
0010b	5 ms <= maximum state duration < 10 ms
0011b	10 ms <= maximum state duration < 50 ms
0100b	50 ms <= maximum state duration < 100 ms
0101b	100 ms <= maximum state duration < 500 ms
0110b	500 ms <= maximum state duration < 1 s
0111b	1 s <= maximum state duration < 5 s
1000b	5 s <= maximum state duration < 10 s
1001b	10 s <= maximum state duration < 1 min
1010b	1 min <= maximum state duration < 5 min
1011b	5 min <= maximum state duration < 10 min
1100b	10 min <= maximum state duration < 50 min
1101b	Maximum state duration >= 50 min
1110b	Reserved
1111b	Reserved

7.4.6 Module Characteristics Advertising

The fields in Table 7-41 describe the characteristics of certain module properties. Some features may be optional. Advertisement of the implementation of optional features is in sections 7.4.7 through 7.4.10. A Tx synchronous group is defined as a Tx input lane or group of Tx input lanes sourced from the same clock domain. Two different Tx synchronous groups may be sourced from different clock domains. There may be a limit on the maximum permissible clock tolerance between two different Tx synchronous groups, as defined by the industry standard associated with a given application code. Refer to applicable industry standards.

A Tx synchronous group can contain one or more data paths, as long as the Tx lanes on all data paths are sourced from the same clock domain and the module takes measures to ensure that active data paths continue to operate undisturbed even as other data paths (and their associated Tx input lanes) are enabled/disabled by the host.

Table 7-41 Module Characteristics Advertising (Page 01h)

Byte	Bit	Name	Description	Type
145	7	Cooling implemented	0b=Uncooled transmitter device 1b=Cooled transmitter	RO RQD
	6-5	Tx input clock recovery capabilities	00b=module requires all Tx input lanes to be in a single Tx synchronous group 11b=module allows each Tx input lane to be in a separate Tx synchronous group	RO RQD
	4	ePPS support	ePPS pin support 0b=ePPS not implemented 1b=ePPS implemented	RO RQD
	3	Select IntL or TxFaultDD	Advertising for supporting signal selection (IntL or TxFaultDD) on pad 22 IntL/TxFaultDD 0b=no signal selection pad 22 only carries IntL if implemented 1b = Signal selection supported (Pad 22 carries IntL or TxFaultDD depending on Byte 26, bit 7) Default value = 0	RO RQD
	2-1	Reserved		
	0	Aux 1 Monitor type	1b=Aux 1 monitor is TEC current 0b=Aux 1 monitor is laser temperature	RO Opt.
146	7-0	Maximum module temperature	Maximum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments. A value of all zeroes indicates not specified.	RO Opt.
147	7-0	Minimum module temperature	Minimum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments**.** A value of all zeroes indicates not specified.	RO Opt.
148	7-0	Propagation Delay MSB	Propagation delay of the non-separable AOC in multiples of 10 ns rounded to the nearest 10 ns. A value of all zeroes indicates not specified.	RO Opt.
149	7-0	Propagation Delay LSB		RO Opt.
150	7-0	Minimum operating voltage	Minimum supported module operating voltage, in 20 mV increments (0 - 5.1 V) A value of all zeroes indicates not specified.	RO Opt.
151	7	Detector type	0b=PIN detector 1b=APD detector	RO RQD
	6-5	Rx Output Eq type	00b=Peak-to-peak amplitude stays constant, or not implemented, or no information 01b=Steady-state amplitude stays constant 10b=Average of peak-to-peak and steady-state amplitude stays constant 11b=Reserved	

Byte	Bit	Name	Description	Type
	4	Rx Optical Power Measurement type	0b=OMA 1b=average power	
	3	Rx LOS type	0b=Rx LOS responds to OMA 1b=Rx LOS responds to Pave	
	2	Rx LOS fast mode implemented	0b=Rx LOS fast mode not implemented 1b=Rx LOS fast mode implemented Refer to form factor hardware specification for timing requirements	
	1	Tx Disable fast mode implemented	0b=Tx Disable fast mode not implemented 1b=Tx Disable fast mode implemented Refer to form factor hardware specification for timing requirements	
	0	Module-Wide Tx Disable	0b=Tx Disable implemented per lane 1b=Any Tx Disable control bit being set disables all Tx lanes	
152	7-0	Per lane CDR Power saved	Minimum power consumption saved per CDR per lane when placed in CDR bypass in multiples of 0.01 W rounded up to the next whole multiple of 0.01 W	RO Opt.
153	7	Rx Output Amplitude code 0011b implemented [1]	0b=Amplitude code 0011b not implemented 1b=Amplitude code 0011b implemented	RO Opt.
	6	Rx Output Amplitude code 0010b implemented [1]	0b=Amplitude code 0010b not implemented 1b=Amplitude code 0010b implemented	
	5	Rx Output Amplitude code 0001b implemented [1]	0b=Amplitude code 0001b not implemented 1b=Amplitude code 0001b implemented	
	4	Rx Output Amplitude code 0000b implemented [1]	0b=Amplitude code 0000b not implemented 1b=Amplitude code 0000b implemented	
	3-0	Max Tx Input Eq	Maximum supported value of the Tx Input Equalization control for manual/fixed programming. (see section 6.2.4.1)	
154	7-4	Max Rx Output Eq Post-cursor	Maximum supported value of the Rx Output Eq Post-cursor control. (see section 6.2.4.2)	RO Opt.
	3-0	Max Rx Output Eq Pre-cursor	Maximum supported value of the Rx Output Eq Pre-cursor control (see section 6.2.4.2)	

Note 1: See Table 6-6

7.4.7 Implemented Controls Advertisement

Table 7-42 describes implemented module and lane controls.

Table 7-42 Implemented Controls Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
155	7	Wavelength control implemented	0b=No wavelength control 1b=Active wavelength control implemented	RO RQD
	6	Tunable transmitter implemented	0b=Transmitter not tunable 1b=Transmitter tunable (page 04h and bank page 12h shall be implemented)	
	5-4	Tx Squelch implemented	00b=Tx Squelch not implemented 01b=Tx Squelch reduces OMA 10b=Tx Squelch reduces Pave 11b=User control, both OMA and Pave squelch supported. (see Table 7-11)	
	3	Tx Force Squelch implemented	0b=Tx Force Squelch not implemented 1b=Tx Force Squelch implemented	
	2	Tx Squelch Disable implemented	0b=Tx Squelch Disable not implemented 1b=Tx Squelch Disable implemented	
	1	Tx Disable implemented	0b=Tx Disable not implemented 1b=Tx Disable implemented	
	0	Tx Polarity Flip implemented	0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented	
156	7-3	Reserved		
	2	Rx Squelch Disable implemented	0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented	RO RQD
	1	Rx Disable implemented	0b=Rx Disable not implemented 1b=Rx Disable implemented	
	0	Rx Polarity Flip implemented	0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented	

7.4.8 Implemented Flags Advertisement

Table 7-43 describes implemented module and lane flags.

Table 7-43 Implemented Flags Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
157	7-4	Reserved		RO RQD
	3	Tx Adaptive Input Eq Failflag implemented	0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented	RO RQD
	2	Tx CDR LOL flag implemented	0b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented	
	1	Tx LOS flag implemented	0b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented	
	0	Tx Fault flag implemented	0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented	
158	7-4	RxLinkUp_MaxDuration	Maximum amount of time that the module may need to provide a valid signal toward the Asic on the host after Rx LOS De-assert (this time includes, for instance, DSP equalization and alignment on the Rx side): in 2 sec increments	
	3	Reserved		RO RQD
	2	Rx LOL flag implemented	0b=Rx CDR Loss of Lock flag not implemented 1b=Rx CDR Loss of Lock flag implemented	RO RQD
	1	Rx LOS flag implemented	0b=Rx Loss of Signal flag not implemented 1b=Rx Loss of Signal flag implemented	
	0	Reserved		RO

7.4.9 Implemented Monitors Advertisement

Table 7-44 describes implemented module and lane monitors.

Table 7-44 Implemented Monitors Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
159	7-3	Reserved		
	2	Aux 1 monitor implemented	0b=Aux 1 monitor not implemented 1b=Aux 1 monitor implemented	RO RQD
	1	Internal 3.3 Volts monitor implemented	0b=Internal 3.3 V monitor not implemented 1b=Internal 3.3 V monitor implemented	
	0	Temperature monitor implemented	0b=Temperature monitor not implemented 1b=Temperature monitor implemented	
160	7-5	Reserved		
	4-3	Tx Bias current measurement and threshold multiplier	Multiplier for 2uA Bias current increment used in Tx Bias current monitor and threshold registers (see Table 7-51 and Table 7-17) 00b=multiply x1 01b=multiply x2 10b=multiply x4 11b=reserved	RO RQD
	2	Rx Optical Input Power monitor implemented	0b=Rx Optical Input Power monitor not implemented 1b=Rx Optical Input Power monitor implemented	
	1	Tx Output Optical Power monitor implemented	0b=Tx Output Optical Power monitor not implemented 1b=Tx Output Optical Power monitor implemented	
	0	Tx Bias monitor implemented	0b=Tx Bias monitor not implemented 1b=Tx Bias monitor implemented	

7.4.10 Implemented Signal Integrity Controls Advertisement

Table 7-45 describes the advertisement of implemented signal integrity controls.

Table 7-45 Implemented Signal Integrity Controls Advertisement(Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Page 01h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

7.4.11 CDB Support Advertisement

Table 7-46 describes the support of the Command Data Block (CDB) and some high-level features therein. Support for specific CDB commands is advertised through the CDB commands shown in Table 7-46. See CMIS for more details on CDB usage.

Table 7-46 CDB Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
163	7-6	CDB implemented	00b=CDB not implemented 01b=Only one instance of CDB implemented. In Pages 9Fh and A0h-AFh, Bank 0 only supported 10b=Two instances of CDB implemented. In Pages 9Fh and A0h-AFh, Bank 0 and 1 supported 11b=Reserved If coded 01b implementation of Byte 8 bit 6 (L-CDB block 1 command complete) flag and associated mask bit (Byte 31 bit 6) is required. If coded 10b implementation of Byte 8 bits 7-6 (L-CDB block 1 and 2 command complete) flags and associated mask bits (Byte 31 bits 7-6) is required.	RO RQD
	5	CDB background operation implemented	0b=Background CDB operation not implemented. The module may NACK after CDB command is triggered, until the command is complete. 1b=Background CDB operation implemented	RO RQD
	4	CDB Auto Paging implemented	When the memory map address pointer advances past the end of an EPL CDB page, the page number will automatically increment and the memory map address pointer will automatically wrap to 128 0b=Auto Paging not implemented 1b=Auto Paging and Auto page wrap implemented	RO RQD
	3-0	Number of EPL Pages implemented	This field defines which EPL pages are implemented in the module and is encoded as follows 0=Pages A0h-AFh not implemented 1=Page A0h implemented, A1h-AFh not implemented 2=Page A0h-A1h implemented, A2h-AFh not implemented 3=Page A0h-A2h implemented, A3h-AFh not implemented 4=Page A0h-A3h implemented, A4h-AFh not implemented 5=Page A0h-A7h implemented, A8h-AFh not implemented 6=Page A0h-ABh implemented, ACh-AFh not implemented 7=Page A0h-AFh implemented The module shall support host reads from and writes to all implemented EPL pages. The behavior of these pages is dependent on the associated CDB command. The advertised Number of EPL Pages Implemented shall be consistent with the pages required for each supported CDB command.	RO RQD
164	7-0	CDB Max TWI Bytes per write transaction	This specification limits the length of TWI write transactions to 8 bytes. This field allows the module to advertise support for longer TWI write transactions, but on CDB pages 9Fh-AFh only. The encoding of this field is as follows: CdbMaxTWIWriteBytes = (Byte 164+1) * 8	RO RQD

Byte	Bit	Name	Description	Type
			A value of 0 indicates that a maximum write length of 8 bytes is permitted. A value of 255 indicates a maximum write length of 2048 bytes is permitted. If the TWI write transaction from the host is longer than the advertised supported max length, the module may ignore bytes that are written beyond the advertised supported max length.	
165	7	CDB command processing option	1b: CDB commands are processed on STOP bit when CMD 128/129 registers are within the write I2C transaction 0b: CDB commands are processed on a write to Byte 129 of Page 9F.	
	6-5	Reserved		
	4-0	CDB commands tNACK time	Denotes tNACK for CDB commands if above 80ms using values of 0-31b. Encoding of tNACK for CDB is this register value*160 ms. The maximum supported tNACK is 4960 ms (Value = 31). This value is ignored when Byte 166 bit 7 is 0b.	
166	7	CDB tNACK time indicator	0b: Indicates that tNACK in bits 6-0 also applies to CDB Generic commands. 1b: Indicates that tNACK in bits 6-0 does not apply to CDB Generic commands. CDB tNACK may be equal to 80 ms or as advertised in Byte 165 Bits 4-0.	
	6-0	Maximum tNACK time	tNACK = (80 - XX) ms. XX is the value of this register in ms. A value of 000 0000b (0) defines modules maximum tNACK of 80 ms. Values of XX>= 80 will be interpreted as having tNACK of 0.	

The CDB Implemented field in page 01h, byte 163, bits 7-6 defines if CDB is supported. If CDB is implemented, this field identifies how many concurrent CDB commands, called CDB instances, are supported in the module. Each CDB instance is associated with a bank number. All CDB instances are expected to behave identically and support the same set of CDB commands. Module support for multiple CDB instances can be useful when long-duration CDB commands are supported, such as firmware update.

The CDB Background Operation Implemented field in byte 163, bit 5 defines if the host may perform other TWI transactions while a CDB command is being executed. If this bit is 0b, the module will NACK while a CDB command is being executed until the command is completed, consistent with the behaviors described in section 5.4.5. If this bit is 1b, the module will NACK until the CDB command is captured. After the command is captured, the module will again respond to TWI transactions. When CDB Background Operation is supported, the host may read the CDB Status field to determine the status of in-progress CDB commands (see Table 7-12). While a CDB Command is being executed in the background, the module shall ensure that any flash writes to code areas do not affect other host interactions with the module that may be occurring in the foreground.

The CDB Auto Paging Implemented (Byte 163, bit 4), Number of EPL pages Implemented (Byte 163, bits 3-0), and CDB Max TWI Bytes Per Write Transaction (Page 01h, Byte 164) fields are interrelated. The module uses these fields to advertise the capabilities of the module. There are some combinations of these fields that should be avoided and some combinations that require further clarification of expected module behaviors. These combinations are described in Table 7-47, below.

Table 7-47 Overview of CDB advertising combinations

CDB Auto Paging impl. (Page 01h, Byte 163, bit 4)	Number of EPL pages impl. (Page 01h, Byte 163, bits 3-0)	CDB Max TWI Bytes per write transaction (Page 01h, Byte 164)	Description
0	Any	<= 128 bytes	This combination is a valid combination and may be advertised. While the host may write up to CDB Max TWI Bytes per write transaction, the host should be careful about writing past the end of the page, since auto paging is not implemented.
0	Any	> 128 bytes	This combination is invalid and should not be advertised, because module behavior for TWI write transactions > 128 bytes is undefined
1	0 or 1 pages	Any	This combination is invalid and should not be advertised, because auto paging is only applicable to multi-page EPL implementations.
1	>= 2 pages	Any	This combination is a valid combination and may be advertised. Since Auto Paging is supported, a TWI write past address 255 will automatically increment the page number and wrap the write address to byte 128. If the host writes past the last implemented EPL page, the page wraps to A0h. If a "page wrap around occurs" the host can no longer read-back the data to compare. The host may use the Auto Paging feature to "stream" data into the module without the overhead of managing page changes.

As an example, the module may advertise a 4 in the Number of EPL Pages Implemented field, indicating support for pages A0-A3h only, but also advertise 255 in the CDB Max TWI Bytes Per Write Transaction field, indicating support for up to 2048 byte writes. This combination is a valid combination. However, since the Max TWI Bytes per write transaction is larger than the number of bytes that can be supported by unique pages, the data written will be accepted by the module but the host may not be able to uniquely read back the data written. To allow for unique read-back of data, the module shall advertise support of a matching number of EPL page bytes and maximum TWI write transaction size.

7.4.12 Additional Durations Advertising

The fields in Table 7-48 advertise module implementation of optional management interface features.

Table 7-48 Additional State Machine Durations Advertising (Page 01h)

Byte	Bit	Name	Description	Type
167	7-4	ModulePwrDn_MaxDuration	Encoded maximum duration of the ModulePwrDn state (see Table 7-40)	RO RQD
	3-0	ModulePwrUp_MaxDuration	Encoded maximum duration of the ModulePwrUp state (see Table 7-40)	
168	7-4	DataPathTxTurnOff_MaxDuration	Encoded maximum duration of the DataPathTxTurnOff state (see Table 7-40)	RO RQD
	3-0	DataPathTxTurnOn_MaxDuration	Encoded maximum duration of the DataPathTxTurnOn state (see Table 7-40)	

These *_MaxDuration fields are defined so host implementers can determine when something has gone wrong in the module during these states, for example a module firmware hang up. These values should be selected to represent the worst-case durations of the applicable state, across all supported configurations. See sections 6.3.1.8 and 6.3.1.10 for details of the ModulePwrUp and ModulePwrDn states and sections 6.3.2.6 and 6.3.2.8 for details of the DataPathTxTurnOn and DataPathTxTurnOff states.

7.4.13 Media Lane Assignment Options Advertising

Each Application descriptor comprises five bytes to advertise an Application, as described in section 6.2.1.1.

The first four bytes are defined in Table 7-24. The fifth byte is defined here in Table 7-49.
Both parts of the application descriptor are linked by the descriptor number known as ApSel Code.

Table 7-49 Media Lane Assignment Advertising (Page 01h)

Byte	Bits	Name	Description	Type
169	7-0	Media Lane Assignment Options, ApSel 0001b	Coded 1 if the Application is allowed to begin on a given media lane. Bits 0-1 correspond to Host Lanes 1-2. In multi-lane Applications each instance of an Application shall use contiguous media lane numbers. If multiple instances of a single Application are allowed each starting point is identified. If multiple instances are advertised, all instance must be supported concurrently. (See section 6.2.1)	RO RQD
170	7-0	Media Lane Assignment Options, ApSel 0010b		
171	7-0	Media Lane Assignment Options, ApSel 0011b		
172	7-0	Media Lane Assignment Options, ApSel 0100b		
173	7-0	Media Lane Assignment Options, ApSel 0101b		
174	7-0	Media Lane Assignment Options, ApSel 0110b		
175	7-0	Media Lane Assignment Options, ApSel 0111b		
176	7-0	Media Lane Assignment Options, ApSel 1000b		

7.4.14 Module-Level Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitor levels where alarms and warnings will be triggered.

Table 7-50 Module-Level Monitor Thresholds (Page 01h)

Byte	Bit	Name	Description	Type
177	7-0	Temperature monitor high alarm threshold MSB	Thresholds for internally measured temperature monitor: signed 2's complement in 1/256 degree Celsius increments	RO Opt.
178	7-0	Temperature monitor high alarm threshold LSB		
179	7-0	Temperature monitor low alarm threshold MSB		
180	7-0	Temperature monitor low alarm threshold LSB		
181	7-0	Temperature monitor high warning threshold MSB		
182	7-0	Temperature monitor high warning threshold LSB		
183	7-0	Temperature monitor low warning threshold MSB		
184	7-0	Temperature monitor low warning threshold LSB		
185	7-0	Supply 3.3-volt monitor high alarm threshold MSB		RO Opt.

Byte	Bit	Name	Description	Type
186	7-0	Supply 3.3-volt monitor high alarm threshold LSB	Thresholds for internally measured 3.3 volt input supply voltage: in 100 µV increments	
187	7-0	Supply 3.3-volt monitor low alarm threshold MSB		
188	7-0	Supply 3.3-volt monitor low alarm threshold LSB		
189	7-0	Supply 3.3-volt monitor high warning threshold MSB		
190	7-0	Supply 3.3-volt monitor high warning threshold LSB		
191	7-0	Supply 3.3-volt monitor low warning threshold MSB		
192	7-0	Supply 3.3-volt monitor low warning threshold LSB		
193	7-0	Aux 1 monitor high alarm threshold MSB	Thresholds for TEC Current or Reserved monitor TEC Current: signed 2's complement in 100/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling	RO Opt.
194	7-0	Aux 1 monitor high alarm threshold LSB		
195	7-0	Aux 1 monitor low alarm threshold MSB		
196	7-0	Aux 1 monitor low alarm threshold LSB		
197	7-0	Aux 1 monitor high warning threshold MSB		
198	7-0	Aux 1 monitor high warning threshold LSB		
199	7-0	Aux 1 monitor low warning threshold MSB		
200	7-0	Aux 1 monitor low warning threshold LSB		
201	7-0	Custom monitor high alarm threshold MSB	Custom monitor: signed or unsigned 16 bit value	RO Opt.
202	7-0	Custom monitor high alarm threshold LSB		
203	7-0	Custom monitor low alarm threshold MSB		
204	7-0	Custom monitor low alarm threshold LSB		
205	7-0	Custom monitor high warning threshold MSB		
206	7-0	Custom monitor high warning threshold LSB		
207	7-0	Custom monitor low warning threshold MSB		
208	7-0	Custom monitor low warning threshold LSB		

7.4.15 Lane-specific Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitor levels where alarms and warnings will be triggered.

Table 7-51 Lane-specific Monitor Thresholds (Page 01h, active modules only)

Byte	Bit	Name	Description	Type
209	7-0	Tx optical power monitor high alarm threshold MSB	Threshold for Tx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 7.2.12 for monitor details including accuracy	RO Opt.
210	7-0	Tx optical power high alarm threshold LSB		
211	7-0	Tx optical power low alarm threshold MSB		
212	7-0	Tx optical power low alarm threshold LSB		
213	7-0	Tx optical power high warning threshold MSB		
214	7-0	Tx optical power high warning threshold LSB		
215	7-0	Tx optical power low warning threshold MSB		
216	7-0	Tx optical power low warning threshold LSB		
217	7-0	Tx bias current monitor high alarm threshold MSB	Threshold for Tx bias monitor: unsigned integer in 2 uA increments, times the multiplier from Table 7-44. See section 7.2.12 for monitor details including accuracy	RO Opt.
218	7-0	Tx bias current high alarm threshold LSB		
219	7-0	Tx bias current low alarm threshold MSB		
220	7-0	Tx bias current low alarm threshold LSB		
221	7-0	Tx bias current high warning threshold MSB		
222	7-0	Tx bias current high warning threshold LSB		
223	7-0	Tx bias current low warning threshold MSB		
224	7-0	Tx bias current low warning threshold LSB		
225	7-0	Rx optical power monitor high alarm threshold MSB	Threshold for Rx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 7.2.12 for accuracy.	RO Opt.
226	7-0	Rx optical power high alarm threshold LSB		
227	7-0	Rx optical power low alarm threshold MSB		
228	7-0	Rx optical power low alarm threshold LSB		
229	7-0	Rx optical power high warning threshold MSB		
230	7-0	Rx optical power high warning threshold LSB		
231	7-0	Rx optical power low warning threshold MSB		
232	7-0	Rx optical power low warning threshold LSB		

7.4.16 Data Path Initialization Control

The DataPathDeinit byte controls the initialization of the lanes in a configured data path This field is ignored when the Module State is not ModuleReady.

The DataPathDeinit bits associated with all lanes in a single data path shall always have the same value. When the Module State is ModuleReady, the data path associated with lanes whose DataPathDeinit bits are set to 0 will transition to the DataPathInit state and begin the initialization process. Refer to section 6.3.2 for details about the Data Path State Machine. The host may deinitialize data paths by setting the appropriate bits to 1. Host implementers should note that, without host intervention, all data paths will begin initializing when the Module State reaches ModuleReady. This auto-initialization behavior can be prevented by writing a 1 to all DataPathDeinit bits when the module is in the ModuleLowPwr state.

Multiple data paths may be initialized or deinitialized at the same time.

The number of lanes in a data path is defined by the selected ApSel Code in the Active Set (see Table 7-20). Refer to section 6.2.1.1 for details on ApSel Codes and section 6.2.3 for details on Control Sets.

Table 7-52 Data Path initialization control (Page 01h)

Byte	Bit	Name	Description	Type
233	7-2	Reserved		RW RQD
	1	DataPathDeinit Host Lane 2	Data Path initialization control for host lane 2 0b=Initialize the data path associated with host lane 2 1b=Deinitialize the data path associated with host lane 2	
	0	DataPathDeinit Host Lane 1	Data Path initialization control for host lane 1 0b=Initialize the data path associated with host lane 1 1b=Deinitialize the data path associated with host lane 1	

7.4.17 Lane-Specific Direct Effect Control Fields

The following fields are provided to control certain properties of individual lanes in the module, independent of the data path. In some cases, behaviors may be overridden by data path characteristics (e.g. Tx Disable in DataPathInit). These settings are not staged and have no relationship to Control Sets.

When a Tx output is disabled, it shall have negligible optical output power (Average power <-20dBm). When a Tx output is squelched and not disabled, either the OMA or the Average power (Pave) is reduced on the optical output (See Table 7-42 and Table 7-11). In cases where both output Disable and Squelch are applied to the same channel, output Disable shall take precedence. If both Disable Tx Squelch and Force Tx Squelch are set for one or more channels, the module shall squelch the channel.

Table 7-53 Lane-specific Control Fields (Page 01h)

Byte	Bits	Name	Description	Type
234	7	Tx2 Polarity Flip	0b=No polarity flip for lane 2 1b=Tx input polarity flip for lane 2	RW Opt.
	6	Tx1 Polarity Flip	0b=No polarity flip for lane 1 1b=Tx input polarity flip for lane 1	
	5	Tx2 Disable	0b=Tx output enabled for media lane 2 1b=Tx output disabled for media lane 2	
	4	Tx1 Disable	0b=Tx output enabled for media lane 1 1b=Tx output disabled for media lane 1	
	3	Tx2 Squelch Disable	0b=Tx output squelch permitted for media lane 2 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 2	
	2	Tx1 Squelch Disable	0b=Tx output squelch permitted for media lane 1 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 1	
	1	Tx2 Force Squelch	0b=No impact on Tx behavior for media lane 2 1b=Tx output squelched for media lane 2	
	0	Tx1 Force Squelch	0b=No impact on Tx behavior for media lane 1 1b=Tx output squelched for media lane 1	
235	7-6	Reserved		RW Opt
	5	Tx2 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 2 1b=Tx input eq adaptation frozen at last value for lane 2	
	4	Tx1 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 1 1b=Tx input eq adaptation frozen at last value for lane 1	
	3-2	Tx2 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4	
	1-0	Tx1 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4	
236	7-6	Reserved		
	5	Rx2 Polarity Flip	0b=No polarity flip for lane 2 1b=Rx output polarity flip for lane 2	RW Opt.
	4	Rx1 Polarity Flip	0b=No polarity flip for lane 1 1b=Rx output polarity flip for lane 1	
	3	Rx2 Output Disable	0b=Rx output enabled for lane 2 1b=Rx output disabled for lane 2	
	2	Rx1 Output Disable	0b=Rx output enabled for lane 1 1b=Rx output disabled for lane 1	
	1	Rx2 Squelch Disable	0b=Rx output squelch permitted for lane 2 1b=Rx output squelch not permitted for lane 2	
	0	Rx1 Squelch Disable	0b=Rx output squelch permitted for lane 1 1b=Rx output squelch not permitted for lane 1	

7.4.18 Staged Control Set 0

Staged Control Set 0 is required for all modules. Refer to section 6.2.3 for background on Control Set methodology.

7.4.18.1 Apply Controls

The host should write the Apply_DataPathInit and Apply_Immediate bytes with one-byte writes. Both bytes are write only. A read of these registers shall return 0.

Table 7-54 Staged Control Set 0, Apply Controls (Page 01h)

Byte	Bits	Name	Description	Type
237	7	Reserved		
	6	Reserved		
	5	Staged Set 0 Lane 2 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 2 settings using DataPathInit	WO RQD
	4	Staged Set 0 Lane 1 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 1 settings using DataPathInit	
	3	Reserved		
	2	Reserved		
	1	Staged Set 0 Lane 2 Apply_Immediate	1b=Apply Staged Control Set 0 lane 2 settings with no Data Path State transitions	WO RQD
	0	Staged Set 0 Lane 1 Apply_Immediate	1b=Apply Staged Control Set 0 lane 1 settings with no Data Path State transitions	

7.4.18.2 Application Select Controls

The following fields allow the host to select one or more of the Applications supported and advertised by the module in Table 7-24. A set of fields is provided for each lane, however Applications that span multiple lanes shall have the same ApSel code and Data Path code for all lanes in the data path. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set.

The ApSel Codes shall be one of the module-advertised ApSel Codes from Table 7-24 or a value of 0000b to indicate that the applicable lane is not part of any data path. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane number would be coded 100b. Explicit Control (bit 0 in bytes 145-152) allows the host to specify signal integrity settings rather than use the Application defined settings. These settings may be specified using Table 7-56 and Table 7-57.

Table 7-55 Staged Control Set 0, Application Select Controls (Page 01h)

Byte	Bits	Name	Description	Type
238	7-4	Staged Set 0 Lane 1 ApSel code	ApSel code from Table 7-24 lane 1	RW RQD
	3-1	Staged Set 0 Lane 1 Data Path ID	First lane of the data path containing lane 1 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 1 Explicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 0 control values for lane 1	
239	7-4	Staged Set 0 Lane 2 ApSel code	ApSel code from Table 7-24 lane 2	RW RQD
	3-1	Staged Set 0 Lane 2 Data Path ID	First lane of the data path containing lane 2 000b=Lane 1, 001b=Lane 2	
	0	Staged Set 0 Lane 2 Explicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 0 control values for lane 2	

7.4.18.3 Tx and Rx Signal Integrity Controls

The following fields allow the host to specify the signal integrity settings for a lane rather than use the defaults associated with the selected Application Code. See section 6.2.3 for the dependency of these fields on the value of the Explicit Control bit. Changes to these fields are not applied until the corresponding lane bits in

Apply_DataPathInit or Apply_Immediate are set. See section 6.2.4 for definitions of valid signal integrity control settings.

Table 7-56 Staged Control Set 0, Tx Controls (Page 01h)

Byte	Bits	Name	Description	Type
240	7-6	Reserved		
	5	Staged Set 0 Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	RW Req
	4	Staged Set 0 Tx1 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	3-2	Staged Set 0 Tx2 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4 for Store/Recall methodology	
	1-0	Staged Set 0 Tx1 Adaptive Input Eq Recall		
241	7-4	Staged Set 0 Tx2 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx1 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
242	7	Reserved		
	6	Reserved		
	5	Staged Set 0 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW
	4	Staged Set 0 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	Req
	3	Reserved		
	2	Reserved		
	1	Staged Set 0 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW
	0	Staged Set 0 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	Req

Table 7-57 Staged Control Set 0, Rx Controls (Page 01h)

Byte	Bits	Name	Description	Type
243	7-4	Staged Set 0 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW
	3-0	Staged Set 0 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	Opt.
244	7-4	Staged Set 0 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW
	3-0	Staged Set 0 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	Opt.
245	7-4	Staged Set 0 Rx2 Output Amplitude control	Rx output amplitude[2]	RW
	3-0	Staged Set 0 Rx1 Output Amplitude control	Rx output amplitude[2]	Opt.

Note 1: See Table 6-5
Note 2: See Table 6-6

7.4.19 Staged Control Set 1

Staged Control Set 1 is MSA optional for all modules but may be needed for some Applications where speed negotiation is performed. The module advertises support for Staged Control Set 1 in Table 7-39. Refer to section 6.2.3 for background on Control Set methodology.

7.4.19.1 Apply Controls

The host should write the Apply_DataPathInit and Apply_Immediate bytes with one-byte writes. Both bytes are write only. A read of these registers shall return 0.

Table 7-58 Staged Control Set 1, Apply Controls (Page 01h)

Byte	Bits	Name	Description	Type
246	7	Reserved		
	6	Reserved		
	5	Staged Set 1 Lane 2 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 2 settings using DataPathInit	WO Opt.
	4	Staged Set 1 Lane 1 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 1 settings using DataPathInit	
	3	Reserved		
	2	Reserved		
	1	Staged Set 1 Lane 2 Apply_Immediate	1b=Apply Staged Control Set 1 lane 2 settings with no Data Path State transitions	WO Opt.
	0	Staged Set 1 Lane 1 Apply_Immediate	1b=Apply Staged Control Set 1 lane 1 settings with no Data Path State transitions	

7.4.19.2 Application Select Controls

The following fields allow the host to select one or more of the Applications supported and advertised by the module in Table 7-24 and Table 8-38. A set of fields is provided for each lane, however Applications that span multiple lanes shall have the same Application code and Data Path code for all lanes in the data path. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set.

The ApSel Codes shall be one of the module-advertised ApSel Codes from Table 7-24 or a value of 0000b to indicate that the applicable lane is not part of any data path. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 2 is the lower lane number would be coded 001b. Explicit Control (bit 0 in bytes 180-187) allows the host to specify signal integrity settings rather than use the Application-defined settings. These settings may be specified using Table 7-60 and Table 7-61.

Table 7-59 Staged Control Set 1, Application Select Controls (Page 01h)

Byte	Bits	Name	Description	Type
247	7-4	Staged Set 1 Lane 1 ApSel code	ApSel code from Table 7-24 lane 1	RW Opt.
	3-1	Staged Set 1 Lane 1 Data Path ID	First lane in the data path containing lane 1 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 1 Explicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 1 control values for lane 1	
248	7-4	Staged Set 1 Lane 2 ApSel code	ApSel code from Table 7-24 lane 2	RW Opt.
	3-1	Staged Set 1 Lane 2 Data Path ID	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 2 Explicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 1 control values for lane 2	

7.4.19.3 Tx and Rx Signal Integrity Controls

The following fields allow the host to specify the signal integrity settings for a lane rather than use the defaults associated with the selected ApSel Code. See section 6.2.3 for the dependency of these fields on the value of the Explicit Control bit. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set. See section 6.2.4 for definitions of valid signal integrity control settings.

Table 7-60 Staged Control Set 1, Tx Controls (Page 01h)

Byte	Bits	Name	Description	Type
249	7-6	Reserved		
	5	Staged Set 1 Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	RW Opt.
	4	Staged Set 1 Tx1 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	3-2	Staged Set 1 Tx2 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4 for Store/Recall methodology	
	1-0	Staged Set 1 Tx1 Adaptive Input Eq Recall		
250	7-4	Staged Set 1 Tx2 Input Eq control	Manual fixed Tx input eq control[1]	RW Opt.
	3-0	Staged Set 1 Tx1 Input Eq control	Manual fixed Tx input eq control[1]	
251	7	Reserved		RW Opt.
	6	Reserved		
	5	Staged Set 1 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 1 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Reserved		
	2	Reserved		
	1	Staged Set 1 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 1 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Note 1: See Table 6-4

Table 7-61 Staged Control Set 1, Rx Controls (Page 01h)

Byte	Bits	Name	Description	Type
252	7-4	Staged Set 1 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
253	7-4	Staged Set 1 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
254	7-4	Staged Set 1 Rx2 Output Amplitude control	Rx output amplitude encoding[2]	RW Opt.
	3-0	Staged Set 1 Rx1 Output Amplitude control	Rx output amplitude encoding[2]	
255	All	Checksum		RO

Note 1: See Table 6-5
Note 2: See Table 6-6

7.4.20 Checksum (Upper Page 01h, Byte 255, RO RQD)

The checksum is a one byte code that can be used to verify that the read-only static data on Page 01h is valid. The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 130 to byte 232, inclusive. Note that the module firmware revision in bytes 128 and 129 is not included in the checksum.

7.5 Page 9Fh (CDB Command Group Summary)

CDB is an optional feature. If CDB is implemented then some commands within each CDB command groups may be required. These registers are intended to be based on the CMIS section 9: (CDB command group summary)

7.6 Page 13h (Module Diagnostics 1)

Upper memory map pages 13h and 14h are banked pages that contain module diagnostic control and status fields. The presence of Page 13h is conditional on the state of bit 5 in Page 01h byte 142 (see Table 7-39). Upper page 13h is subdivided into several areas as illustrated in the following table:

Table 7-62 Page 13h Overview

Byte	Size (bytes)	Name	Description
128	1	Loopback capabilities	Module advertisement
129	1	General pattern capabilities	Module advertisement
130	1	Diagnostic reporting capabilities	Module advertisement
131	1	Pattern Generation and Checking locations	Module advertisement
132-142	11	Pattern Generation and Checking capabilities	Module advertisement
143	1	Reserved	Reserved for Module advertisement
144-151	8	Pattern Generator, host side	Host controls
152-159	8	Pattern Generator, media side	Host controls
160-167	8	Pattern Checker, host side	Host controls
168-175	8	Pattern Checker, media side	Host controls
176-179	4	General Generator/Checker controls	Host controls
180-183	4	Loopback controls	Host controls
184-195	12	Reserved	
196-205	10	Custom	
206-223	18	Diagnostic flag masks	Page 14h Flags in bytes 132-149
224-255	32	User Pattern	

7.6.1 Loopback Capabilities Advertisement

Four different types of loopback are defined by this specification and Figure 7-3 illustrates each loopback types.

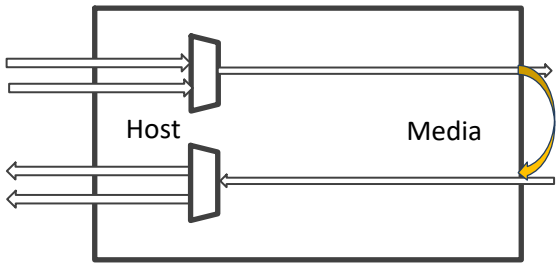
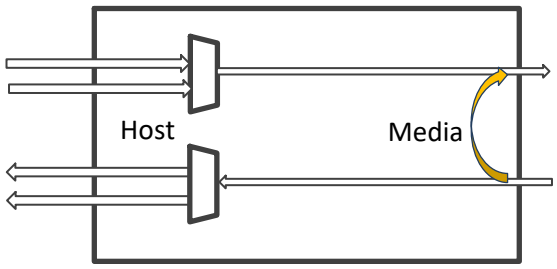
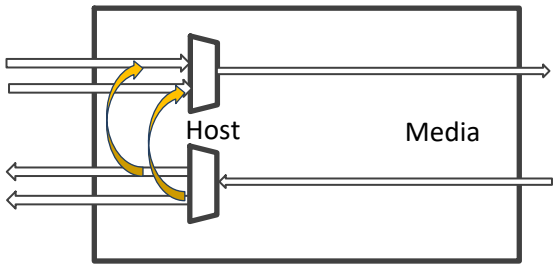
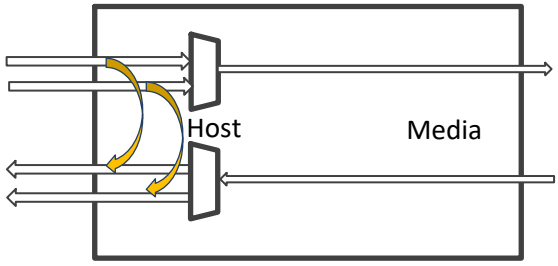
Name	Illustration
Media Side Output Loopback (only one host lane shown)	
Media Side Input Loopback (only one media lane shown)	
Host Side Output Loopback (only one media lane shown)	
Host Side Input Loopback (only one host lane shown)	

Figure 7-3 Loopback Type Illustrations

The loopback capabilities of the module are advertised in Table 7-63.

Table 7-63 Loopback Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
128	7	Reserved		
	6	Simultaneous Host and Media Side Loopback supported	0b=Simultaneous host and media side loopback not supported 1b=Simultaneous host/media side loopback supported	RO RQD
	5	Per-lane Media Side Loopback supported	0b=Individual lane media side loopback not supported 1b=Individual lane media side loopback supported	
	4	Per-lane Host Side Loopback supported	0b=Individual lane host side loopback not supported 1b=Individual lane host side loopback supported	
	3	Host Side Input Loopback supported	0b=Host side input loopback not supported 1b=Host side input loopback supported	
	2	Host Side Output Loopback supported	0b=Host side output loopback not supported 1b=Host side output loopback supported	
	1	Media Side Input Loopback supported	0b=Media side input loopback not supported 1b=Media side input loopback supported	
	0	Media Side output Loopback supported	0b=Media side output loopback not supported 1b=Media side output loopback supported	

7.6.2 General Pattern Capabilities Advertisement

The general pattern generator/checker capabilities of the module are advertised in Table 7-64.

Table 7-64 General Pattern Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
129	7-6	Gating Supported	00b=Not Supported 01b=Supported with time accuracy <= 2 ms 10b=Supported with time accuracy <= 20 ms 11b=Supported with time accuracy > 20 ms Total bits can be used to denote time, unless BER registers are used	RO RQD
	5	Latched Error Information Supported	Latched Error Information in Page 14h.Byte128 Selectors 11h-15h support advertisement. 0b=Not Supported. 1b=Supported.	
	4	Real-time BER Error Count Polling by Module	This flag controls if the module polls and updates the error information BER or Total Error Counters. Non-Gating Mode. 0b: Module does not poll Error Information. 1b: Module polls error information at update rate defined by 13h.Byte177.Bit0. Gating Mode. 0b: Modules does not poll Error Information. At the end of the gating period, the error counters are updated. If latched selectors 11h-15h are implemented these latched error counters will also be updated. 1b: Module Error Information is updated whilst Gating is in progress. Update time defined by Byte 177 Bit 0.	
	3	Per Lane Gating Timer	0b=One gating timer supported Host PRBS Checker and One Gating timer for Media PRBS Checkers is available for all lanes all banks. Two timers in totality. 1b=Per lane gating timer supported.	
	2	Auto Restart Implemented	0b=Auto Restart not implemented 1b=Auto Restart implemented.	
	1-0	Reserved	Reserved	

7.6.3 Diagnostic Reporting Capabilities Advertisement

The diagnostic reporting capabilities of the module are advertised in Table 7-65.

Table 7-65 Diagnostic Reporting Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
130	7	Media side FEC supported	1b=Supported 0b=Not supported	RO RQD
	6	Host side FEC supported	1b=Supported 0b=Not supported	
	5	Media side input SNR measurement supported	Indicates if a Diagnostics Selection value of 09h is supported (Page 14h byte 128, Table 7-87) 1b=Supported 0b=Not supported	
	4	Host side input SNR measurement supported	Indicates if a Diagnostics Selection value of 08h is supported (Page 14h byte 128, Table 7-87) 1b=Supported 0b=Not supported	
	3	Reserved		
	2	Reserved		
	1	BER Error Count/Total Bits supported	Indicates if a Diagnostics Selection values of 02h-05h are supported (Page 14h byte 128, Table 7-87) 1b=Supported 0b=Not supported Some modules are unable to perform a 64 bit division to calculate and present BER. It is expected these types of module will present the BER as error counts and total bits elapsed for the error counts presented. *For data coherency requirements see Section 5.4.2.*	RO RQD
	0	BER register supported	Indicates if a Diagnostics Selection value of 01h is supported (Page 14h byte 128, Table 7-87) 1b=Supported 0b=Not supported	

7.6.4 Pattern Generation and Checking Location Advertisement

The locations of PRBS generators, checkers and FEC functions are advertised in Table 7-66. A reference diagram showing the possible locations for PRBS generators, checkers and FEC functions is shown in Figure 7-4. The FEC block functionality is determined by the interface ID. (See SFF-8024)

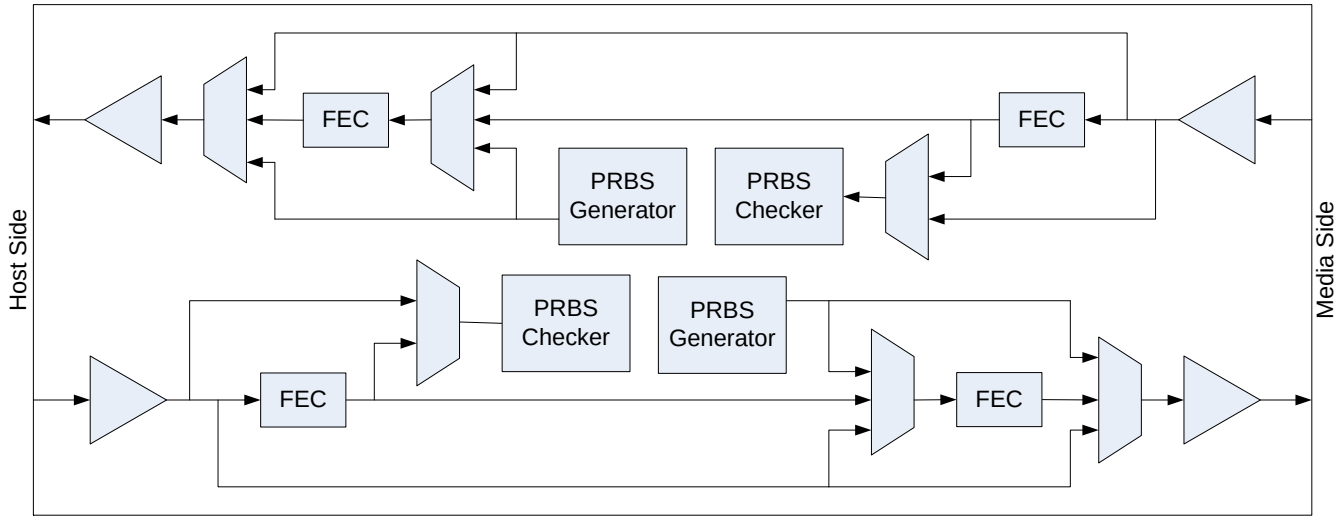


Figure 7-4 PRBS Paths Reference Diagram

Table 7-66 Pattern Generation and Checking Location (Page 13h)

Byte	Bits	Name	Description	Type
131	7	Media side pre-FEC PRBS generator supported	1b=Supported 0b=Not supported	RO RQD
	6	Media side post-FEC PRBS generator supported		
	5	Media side pre-FEC PRBS checker supported		
	4	Media side post-FEC PRBS checker supported		
	3	Host side pre-FEC PRBS generator supported		
	2	Host side post-FEC PRBS generator supported		
	1	Host side pre-FEC PRBS checker supported		
	0	Host side post-FEC PRBS checker supported		

7.6.5 Pattern Generation and Checking Capabilities Advertisement

This specification defines sixteen unique patterns that can be generated and/or checked by the module. These patterns are coded according to Table 7-67. All patterns with names ending in 'Q' are defined for PAM4 modulation using Gray coding. See section 3.3 for definition of Gray coding. The signal rate for these patterns is determined by the selected Application code for the associated lane.

Table 7-67 Pattern coding

PRBS Pattern code	Name	Description
0	PRBS-31Q	As defined in 802.3-2018 clause 120.5.11.2.2
1	PRBS-31	
2	PRBS-23Q	ITU-T Recommendation O.172, 2005
3	PRBS-23	
4	PRBS-15Q	x^15 + x^14 + 1
5	PRBS-15	
6	PRBS-13Q	As defined in 802.3-2018 clause 120.5.11.2.1
7	PRBS-13	
8	PRBS-9Q	As defined in 802.3-2018 clause 120.5.11
9	PRBS-9	
10	PRBS-7Q	x^7 + x^6 + 1
11	PRBS-7	
12	SSPRQ	As defined in 802.3-2018 clause 120.5.11.2.3
13	Reserved	
14	Custom	Vendor Pattern
15	User Pattern	Pattern provided in bytes 224-255

The pattern generation capabilities of the module are advertised in Table 7-68. The pattern number corresponds to the pattern coding in Table 7-67.

Table 7-68 PRBS Pattern Generation Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
132	7	Host Side Generator Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Generator Pattern 6 supported		
	5	Host Side Generator Pattern 5 supported		
	4	Host Side Generator Pattern 4 supported		
	3	Host Side Generator Pattern 3 supported		
	2	Host Side Generator Pattern 2 supported		
	1	Host Side Generator Pattern 1 supported		
	0	Host Side Generator Pattern 0 supported		
133	7	Host Side Generator Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Generator Pattern 14 supported		
	5	Host Side Generator Pattern 13 supported		
	4	Host Side Generator Pattern 12 supported		
	3	Host Side Generator Pattern 11 supported		
	2	Host Side Generator Pattern 10 supported		
	1	Host Side Generator Pattern 9 supported		
	0	Host Side Generator Pattern 8 supported		
134	7	Media Side Generator Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Generator Pattern 6 supported		
	5	Media Side Generator Pattern 5 supported		
	4	Media Side Generator Pattern 4 supported		
	3	Media Side Generator Pattern 3 supported		
	2	Media Side Generator Pattern 2 supported		
	1	Media Side Generator Pattern 1 supported		
	0	Media Side Generator Pattern 0 supported		
135	7	Media Side Generator Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Generator Pattern 14 supported		
	5	Media Side Generator Pattern 13 supported		
	4	Media Side Generator Pattern 12 supported		
	3	Media Side Generator Pattern 11 supported		
	2	Media Side Generator Pattern 10 supported		
	1	Media Side Generator Pattern 9 supported		
	0	Media Side Generator Pattern 8 supported		

The pattern checking capabilities of the module are advertised in Table 7-69. The pattern number corresponds to the pattern coding in Table 7-67.

Table 7-69 Pattern Checking Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
136	7	Host Side Checker Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Checker Pattern 6 supported		
	5	Host Side Checker Pattern 5 supported		
	4	Host Side Checker Pattern 4 supported		
	3	Host Side Checker Pattern 3 supported		
	2	Host Side Checker Pattern 2 supported		
	1	Host Side Checker Pattern 1 supported		
	0	Host Side Checker Pattern 0 supported		
137	7	Host Side Checker Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Checker Pattern 14 supported		
	5	Host Side Checker Pattern 13 supported		
	4	Host Side Checker Pattern 12 supported		
	3	Host Side Checker Pattern 11 supported		
	2	Host Side Checker Pattern 10 supported		
	1	Host Side Checker Pattern 9 supported		
	0	Host Side Checker Pattern 8 supported		
138	7	Media Side Checker Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Checker Pattern 6 supported		
	5	Media Side Checker Pattern 5 supported		
	4	Media Side Checker Pattern 4 supported		
	3	Media Side Checker Pattern 3 supported		
	2	Media Side Checker Pattern 2 supported		
	1	Media Side Checker Pattern 1 supported		
	0	Media Side Checker Pattern 0 supported		
139	7	Media Side Checker Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Checker Pattern 14 supported		
	5	Media Side Checker Pattern 13 supported		
	4	Media Side Checker Pattern 12 supported		
	3	Media Side Checker Pattern 11 supported		
	2	Media Side Checker Pattern 10 supported		
	1	Media Side Checker Pattern 9 supported		
	0	Media Side Checker Pattern 8 supported		

Additional pattern capabilities are advertised in Table 7-70.

Table 7-70 Pattern Generator and Checker swap and invert Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
140	7-6	Recovered Clock can be used for pattern generator	00b:Recovered clock for generator not supported 01b:Supports Recovered clock pattern normal path 10b:Supports Recovered clock pattern loopback path. 11b:Supports both, selection made as function of loopback	RO RQD
	5	Reference Clock	Since this is the diagnostics page, the Reference clock bit here only controls reference clock in relation to diagnostics and not module operation. 1b:Reference Clock is available for patterns 0b:Reference Clock is not available for patterns	
	4-0	User Pattern supported length	Maximum length of the user pattern, in 2 byte increments. 0000b=2 bytes, 1111b=32 bytes	
141	7	Media Side Checker Data Swap	0b: Page 13h.Byte170 not supported. 1b: Page 13h.Byte170 supported.	RO RQD
	6	Media Side Checker Data Invert	0b: Page 13h.Byte169 not supported. 1b: Page 13h.Byte169 supported.	
	5	Media Side Generator Data Swap	0b: Page 13h.Byte154 not supported. 1b: Page 13h.Byte154 supported.	
	4	Media Side Generator Data Invert	0b: Page 13h.Byte153 not supported. 1b: Page 13h.Byte153 supported.	
	3	Host Side Checker Data Swap	0b: Page 13h.Byte162 not supported. 1b: Page 13h.Byte162 supported.	
	2	Host Side Checker Data Invert	0b: Page 13h.Byte161 not supported. 1b: Page 13h.Byte161 supported.	
	1	Host Side Generator Data Swap	0b: Page 13h.Byte146 not supported. 1b: Page 13h.Byte145 supported.	
	0	Host Side Generator Data Invert	0b: Page 13h.Byte145 not supported. 1b: Page 13h.Byte145 supported.	
142	7	Media Checker Per lane Enables	Media Side pattern checker can be enable per lane at a time or all lanes will be enable. (13h.Byte168) 0b: per lane enable not supported. 1b: per lane enable supported.	RO RQD
	6	Media Checker Per Lane Pattern Type Selection	Media Side pattern checker type configuration. 0b: Pattern Type 13h.Byte172.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte172-175.	
	5	Media Generator Per lane Enables	Media Side pattern generator can be enable per lane at a time or all lanes will be enable. (13h.Byte152) 0b: per lane enable not supported. 1b: per lane enable supported.	
	4	Media Generator Per Lane Pattern Type Selection	Media Side pattern checker type configuration. 0b: Pattern Type 13h.Byte156.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte156-159.	
	3	Host Checker Per lane Enables	Host Side pattern checker can be enable per lane at a time or all lanes will be enable. (13h.Byte160) 0b: per lane enable not supported. 1b: per lane enable supported.	
	2	Host Checker Per Lane Pattern Type Selection	Host Side pattern checker type configuration. 0b: Pattern Type 13h.Byte164.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte164-167.	
	1	Host Generator Per lane Enables	Host Side pattern generator can be enable per lane at a time or all lanes will be enable. (13h.Byte144) 0b: per lane enable not supported.	

Byte	Bits	Name	Description	Type
			1b: per lane enable supported.	
	0	Host Generator Per Lane Pattern Type Selection	Host Side pattern checker type configuration. 0b: Pattern Type 13h.Byte148.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte148-151.	
143	7-0	Reserved		

7.6.6 Host Side Pattern Generator Controls

The controls in this section control pattern generation on the host side of the module, also known as the Rx electrical output.

Table 7-71 defines the host side pattern generator controls and Table 7-72 defines the host side pattern generator selection controls.

Table 7-71 Host Side Pattern Generator Controls (Page 13h)

Byte	Bits	Name	Description	Type
144	7	Reserved	1b=Enable generator, using the configuration defined in bytes 145-151 0b=Disable pattern generator	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Reserved		
	0	Reserved		
145	7	Reserved	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap is controlled by the polarity controls in Table 7-53	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host Side Generator Lane 2 data invert		
	0	Host Side Generator Lane 1 data invert		
146	7	Reserved	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host Side Generator Lane 2 byte swap		
	0	Host Side Generator Lane 1 byte swap		
147	7	Reserved	1b=Generate the selected pattern at the input to the internal FEC block 0b= Generate the selected pattern at the output from the internal FEC block	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host Side Generator Lane 2 pre-FEC enable		
	0	Host Side Generator Lane 1 pre-FEC enable		

Table 7-72 Host Side Pattern Generator Select Controls (Page 13h,)

Byte	Bits	Name	Description	Type
148	7-4	Host Side Generator Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 7-67 for pattern codings.	RW Opt.
	3-0	Host Side Generator Lane 1 pattern select		
149	7-4	Reserved		
	3-0	Reserved		
150	7-4	Reserved		
	3-0	Reserved		
151	7-4	Reserved		
	3-0	Reserved		

7.6.7 Media Side Pattern Generator Controls

The controls in this section control pattern generation on the media side of the module, also known as the Tx electrical or optical output. Table 7-73 defines the media side pattern generator controls and Table 7-74 defines the media side pattern generator selection controls.

Table 7-73 Media Side Pattern Generator Controls (Page 13h)

Byte	Bits	Name	Description	Type
152	7	Reserved	1b=Enable generator, using the configuration defined in bytes 153-159 0b=Disable pattern generator	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Generator Lane 2 enable		
	0	Media Side Generator Lane 1 enable		
153	7	Reserved	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap is controlled by the polarity controls in Table 7-53	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Generator Lane 2 data invert		
	0	Media Side Generator Lane 1 data invert		
154	7	Reserved	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Generator Lane 2 byte swap		
	0	Media Side Generator Lane 1 byte swap		
155	7	Reserved	1b=Generate the selected pattern at the input to the internal FEC block 0b= Generate the selected pattern at the output from the internal FEC block	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Generator Lane 2 pre-FEC enable		
	0	Media Side Generator Lane 1 pre-FEC enable		

Table 7-74 Media Side Pattern Generator Select Controls (Page 13h)

Byte	Bits	Name	Description	Type
156	7-4	Media Side Generator Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 7-67 for pattern codings.	RW Opt.
	3-0	Media Side Generator Lane 1 pattern select		
157	7-4	Reserved		
	3-0	Reserved		
158	7-4	Reserved		
	3-0	Reserved		
159	7-4	Reserved		
	3-0	Reserved		

7.6.8 Host Side Pattern Checker Controls

The controls in this section control pattern checking on the host side of the module, also known as the Tx electrical input. Table 7-75 defines the host side pattern checker controls and Table 7-76 defines the host side pattern checker selection controls.

Table 7-75 Host Side Pattern Checker Controls (Page 13h)

Byte	Bits	Name	Description	Type
160	7	Reserved	1b=Enable checker, using the configuration defined in bytes 161-167 0b=Disable pattern checker	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host Side Checker Lane 2 enable		
	0	Host Side Checker Lane 1 enable		
161	7	Reserved	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap for input signals is not currently supported by this specification.	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host Side Checker Lane 2 data invert		
	0	Host Side Checker Lane 1 data invert		
162	7	Reserved	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host Side Checker Lane 2 byte swap		
	0	Host Side Checker Lane 1 byte swap		
163	7	Reserved	1b=Check the selected pattern at the output from the internal FEC block 0b=Check the selected pattern at the input to the internal FEC block	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host Side Checker Lane 2 post-FEC enable		
	0	Host Side Checker Lane 1 post-FEC enable		

Table 7-76 Host Side Pattern Checker Select Controls (Page 13h)

Byte	Bits	Name	Description	Type
164	7-4	Host Side Checker Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 7-67 for pattern codings.	RW Opt.
	3-0	Host Side Checker Lane 1 pattern select		
165	7-4	Reserved		
	3-0	Reserved		
166	7-4	Reserved		
	3-0	Reserved		
167	7-4	Reserved		
	3-0	Reserved		

7.6.9 Media Side Pattern Checker Controls

The controls in this section control pattern checking on the media side of the module, also known as the Rx electrical or optical input. Table 7-77 defines the media side pattern checker controls and Table 7-78 defines the media side pattern checker selection controls.

Table 7-77 Media Side Pattern Checker Controls (Page 13h)

Byte	Bits	Name	Description	Type
168	7	Reserved	1b=Enable checker, using the configuration defined in bytes 169-175 0b=Disable pattern checker	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Checker Lane 2 enable		
	0	Media Side Checker Lane 1 enable		
169	7	Reserved	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap for input signals is not currently supported by this specification.	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Checker Lane 2 data invert		
	0	Media Side Checker Lane 1 data invert		
170	7	Reserved	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Checker Lane 2 byte swap		
	0	Media Side Checker Lane 1 byte swap		
171	7	Reserved	1b=Check the selected pattern at the output from the internal FEC block 0b=Check the selected pattern at the input to the internal FEC block	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media Side Checker Lane 2 post-FEC enable		
	0	Media Side Checker Lane 1 post-FEC enable		

Table 7-78 Media Side Pattern Checker Select Controls (Page 13h)

Byte	Bits	Name	Description	Type
172	7-4	Media Side Checker Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 7-67 for pattern codings.	RW Opt.
	3-0	Media Side Checker Lane 1 pattern select		
173	7-4	Reserved		
	3-0	Reserved		
174	7-4	Reserved		
	3-0	Reserved		
175	7-4	Reserved		
	3-0	Reserved		

7.6.10 General Generator/Checker Controls

Table 7-79 provides general controls for the pattern generator and checker features. For examples of the usage of the Generator/Checker Controls see Appendix C.

Table 7-79 General Generator/Checker Controls (Page 13h)

Byte	Bits	Name	Description	Type
176	7-4	Host PRBS Generator Clock Source	The source of the clock to be that is used for Host PRBS Pattern Generation can be configured using this control register. The following selection options are defined. 0h:All lanes uses Internal Clock 1h:All lanes uses Reference Clock 2h:All lanes uses Recovered Clock Media Lane 1 3h:All lanes uses Recovered Clock Media Lane 2 Ah-Eh: Reserved. Fh: Recovered clock from Respective Media Lane/Datapaths are used.	RW Opt.
	3-0	Media PRBS Generator Clock Source	The source of the clock to be that is used for Media PRBS Pattern Generation can be configured using this control register. The following selection options are defined. 0h:All lanes uses Internal Clock 1h:All lanes uses Reference Clock 2h:All lanes uses Recovered Clock Host Lane 1 3h:All lanes uses Recovered Clock Host Lane 2 Ah-Eh: Reserved. Fh: Recovered clock from Respective Host Lane/Datapaths are used.	
177	7	Reset all lanes	This bit controls the behavior of the "Reset Error Counters" or "Enabling and Disabling PRBS checker lanes", whether the operation applies to enabled lanes within a bank or enabled lanes in all banks with this bit set to 1b. 0b: Applies to individual lane/bank. 1b: Applies to all lanes all banks with this bit=1. Whenever a reset error information operation on and individual lane or all lanes are triggered, it should always clear Error Information (both PRBS BER and Error Counters) at the same time.	RW Opt.
	6	Reserved		
	5	Reset Error Information	Whenever this bit is set to 1b, the Error Information in Selector 01h to 05h are frozen and if implemented 11h-15h will be updated with the Error Information. Whenever this bit is set to 0b, Error Information in Selectors 01h-05h will be reset to 0. Selectors 11h-15h will not be affected by this bit setting to 0. Furthermore, the behavior of this bit depends on the configuration 13h.Byte129.Bit3 and register 13h.Byte177.Bit7 as well as the Gating Mode 13h.Byte177.Bit3-1.	

Byte	Bits	Name	Description	Type
			When configuration in 13h.Byte129.Bit3=0, there is only 1 timer for all lane and all banks. Setting this bit to 1b will keep the gate timers reset. Setting this bit to 0b will start the single gating timer. When configuration 13h.Byte129.Bit3=1, there are individual timers per lane (in all banks). Setting this bit to 1b will keep the gate timers reset for the lanes in this bank only if 13h.Byte177.Bit7=0. Setting this bit to 0b will start the individual gating timers for all enabled lanes in this bank.	
	4	Auto Restart Gate Time	0b=When Gate Time expires, the module will set the Gate Complete Flag in Page 14h, bytes 134-135. The module will update the latched error counters and stop error detection. 1b=When Gate Time expires, the module will set the Gate Complete Flag in Page 14h, bytes 134-135. The module will update the latched error counters, then immediately clear internal error counters and restart the Gate Timer, while continuing to count errors. The host must read the latched error counters before the Gate Time expires to avoid the values being overwritten with new counts.	
	3-1	Gate Time	The pattern checker will stop accumulating errors after this gate time has elapsed. 000b=not gated, counters accrue indefinitely 001b=5 sec gate time 010b=10 sec gate time 011b=30 sec gate time 100b=60 sec gate time 101b=120 sec gate time 110b=300 sec gate time 111b=Custom	
	0	BER/Error Count Update time	If configured (see Table 7-64) Page 13h Byte 129 Bit 4 when set to 1b advertises that the module will be able to update the BER or Error counters whilst gating is in progress. Two update rates at which the module will process the internal error counters and update the error counter fields in the memory map are possible. If gating is enabled, the host can poll error registers for cumulative "real-time" error counts, up until the first gate is reached. 0b=1 sec update interval 1b=5 sec update interval *For data coherency requirements see Section 5.4.2.*	
178	7-4	Reserved		
	3-2	Host PRBS Checker Clock Source	The source of the clock that is used for the Host PRBS Pattern Checker can be configured using this control register. The following selection options are defined. 0h: Recovered clocks from Respective Host Lane/Datapaths are used. 1h: All lanes use Internal Clock. 2h: All lanes use Reference Clock 3h: Reserved.	RW
	1-0	Media PRBS Checker Clock Source	The source of the clock that is used for the Media PRBS Pattern Checker can be configured using this control register. The following selection options are defined. 0h: Recovered clocks from Respective Media Lane/Datapaths are used. 1h: All lanes use Internal Clock. 2h: All lanes use Reference Clock 3h: Reserved.	RW
179	7-0	Reserved		

7.6.10.1 PRBS Controls and Behavior Un-Gated Mode

These section describes the behavior specifically related to behavior of the PRBS Checkers and error information registers when 13h.Byte177.Bits3-1 is 000b. The PRBS error information accessed by the selector byte Page 14h.Byte128 and information Bytes 192-255 will be referenced in the following table below. Furthermore the configuration of Page 13h.Byte129.Bit4 defines the behavior of the module availability of the real-time error information.

The COR flags in Page 14h.Bytes 134-135 will be not raised is this un-gated PRBS checker mode and the host will have to poll the error information registers.

Table 7-80 PRBS Checker Behavior Un-Gated Mode

Required Mode of Operation	Byte 177 (D7-D0)	Description
Bit 3-1=000b. Not-Gated (Hence Bit 4 ignored) All lanes control bit 7=0.	0000 000y *nnn* = 000	In this mode, the error information BER and error counters are running continuously. Whenever PRBS Enable Bits in Page 13h Byte/s 160 or 168 are enabled by TWI write, all error counters for the enable lanes will reset to 0 and start accumulating errors. PRBS Error counters are stopped when the host disables the PRBS Error Checker Bytes 160 or 168, at which time the error information of prior to disabled will be available in the Selector 01-05h and the module shall present the last error information in both the Selector 01h-05h (and 11h-15h if implemented). If 13h.Byte129.Bit4 = 0, real time error information are not updated. The error information will only available when the PRBS enable bits on Byte 160 or 168 are disabled. If 13h.Byte129.Bit4 = 1, real time error information are available by using Page 14h using the Selectors 01h-05h. These real time error information will be updated by the module every configure "y" seconds. Accurate error counter accumulation times can be derived from the total bit counters in the error information. A write to 13h.Byte177.Bit5=1 will also cause the error information registers to reset to 0 and restart accumulation on the enabled lanes.
Bit 3-1=000b. Not-Gated (Hence Bit 4 ignored) All lanes control bit 7=1.	100x 000y *nnn* = 000	The behavior with is the same as the above row with the exception that when a write to 13h.Byte177.Bit5=1 the error information registers of **all lanes in all banks** (since 13h.Byte177.Bit7=1) will be reset to 0 and restart accumulation. As described above just prior to reset of error information of all lanes in all banks, the previous error information should be copied to both 01-05h (and 11h-15h if implemented). Selector 01-05h will restart accumulation and 11h-15h if implemented will contain the latched error information of the previous period prior to reset.
Reset Error Counters (Bit 5) Since 13h.Byte129.Bit3=0 there is only one timer for host and one timer for media lanes. Hence 13h.Byte177.Bit7 has no relevance.	x010 nnny nnn = 000	This bit is used to clear the error counters and restart accumulation of errors. When 13h.Byte177.Bit5 is set to 1b, all the enabled lanes error counters are frozen from the previous state and available from reading Selectors 01h-05h (and 11h-15h if implemented). When 13h.Byte177.Bit5 is set to 0b, all the error information of enabled PRBS checker of both host and media lanes are reset to 0. The host may also individually toggle Host Byte 160 or Media Byte 168 enable bits to restart the error information of the lanes independently.

7.6.10.2 PRBS Controls and Behavior – Single Gate Timer

These section describes the behavior specifically related to behavior of the module when Page 13h.Byte129.Bit3 is 0 indicating that there is only one Gate Timer for all channels and all banks. The PRBS error information accessed by the selector byte Page 14h.Byte128 and information Bytes 192-255 will be referenced in the following table below. Furthermore the configuration of Page 13h.Byte129.Bit4 defines the behavior of the module availability of the real-time error information whilst the gating timer is running and has not expired.

In the following table whenever gating is enabled, the COR flags in Page 14h.Bytes 134-135 will be raised as well as IntL may be asserted at the expiry of the gate timers to indicate that error information registers are available. If the host fails to read the error information registers prior to expiry of subsequent gate time expiry, only the latest error information will be available.

Table 7-81 PRBS Checker Behavior Single Gate Timer

Required Mode of Operation	Byte 177 (D7-D0)	Description
Gated, nnn configured secs. Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored.	X000 *nnn*y *nnn* != 000	PRBS Error Counters are gated. Whenever PRBS Enable Bits in Page 13h Byte/s 160 or 168 are enabled by TWI write, the respective Host or Media single gate timer will reset to 0, all error counters for the enable lanes will reset to 0 and start accumulating errors. At the end of the gate, that is when the gate timer expires and exceeds the "nnn" elapsed time configured seconds, the PRBS Error counters will stop counting. At this time the module shall be able to present the error information collected within this gating period on Page 14h by using the Selectors 01h-05h (and 11h-15h if implemented). If 13h.Byte129.Bit4 = 0, real time error information are not updated whilst gating is in progress. The error information will only available at the end of the gate. If 13h.Byte129.Bit4 = 1, real time error information are available by using Page 14h using the Selectors 01h-05h. These real time error information will be updated by the module every configure "y" seconds. This mode is useful if the gating period is long. A host may choose to periodically read the real-time error information during gating and take any necessary action if a bad BER is detected. To restart gating, the host has to toggle the PRBS enable registers 160 and 168.
Gated, nnn configured secs. Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored. If the Page 13h.Byte129.Bit2 is set, and the host writes a 1 to Bit4 of Byte 177, the gating timer will automatically restart.	xx01 *nnn*y *nnn* != 000	This behavior is the same as the above row, except for the behavior when the gate timer expires and exceeds the configured gate time. Module should support Selectors 11h-15h to use this feature, otherwise error information from the previous gating period will be lost. Here at the end of the gate, that is when the gate timer expires and exceeds the configured "nnn" elapsed time, the PRBS error information will be presented in the latched error information via the Selectors 11h-15h. The current error information will reset and the gate timer will be reset to 0 and restart accumulating errors for a new gating period. The host will have to read the

Required Mode of Operation	Byte 177 (D7-D0)	Description
		error information from the previous gated time using the latched error information Selectors 11h-15h.
Restart gate timer (Bit 5) Since 13h.Byte129.Bit3=0 there is only one timer for host and one timer for media lanes. Hence 13h.Byte177.Bit7 has no relevance.	x01x *nnn*y *nnn* != 000	This bit is used to restart the both the single host and media gate timers. When Byte177.Bit5 is set to 1b, all the enabled lanes error counters are frozen from the previous state and the gate timers are stopped. When Byte177.Bit5 is set to 0b, both the host and media enabled the gate timers are restarted from 0 and the error information are reset and a new error accumulation gate period is restarted. The host may also individually toggle host Byte 160 or media Byte 168 enable bits to restart the gate timer for the host and media lanes independently.

7.6.10.3 PRBS Controls and Behavior – Per Lane Gate Timer

These section describes the behavior specifically related to behavior of the module when Page 13h.Byte129.Bit3 is 1 indicating that there are individual lanes Gate Timer for all channels and all banks. The PRBS error information accessed by the selector byte Page 14h.Byte128 and information Bytes 192-255 will be referenced in the following table below. Furthermore the configuration of Page 13h.Byte129.Bit4 defines the behavior of the module availability of the real-time error information whilst the gating timer is running and has not expired.

In the following table whenever gating is enabled, the COR flags in Page 14h.Bytes 134-135 will be raised as well as IntL may be asserted at the expiry of the gate timers to indicate that error information registers are available. If the host fails to read the error information registers prior to expiry of subsequent gate time expiry, only the latest error information will be available.

Table 7-82 PRBS Checker Behavior Per Lane Gate Timer

Required Mode of Operation	Byte 177 (D7-D0)	Description
Gated, nnn configured secs. Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored.	X000 *nnn*y *nnn* != 000	PRBS Error Counters are gated. Whenever PRBS Enable Bits in Page 13h Byte/s 160 or 168 are enabled by TWI write, the respective Host or Media lane gate timer will reset to 0, all error counters for the enable lanes will reset to 0 and start accumulating errors. Since there are individual per lane gate timers, these timers should reset independently to provide the most accurate per lane gated time as possible. At the end of the gate, that is when the gate timer expires and exceeds the "nnn" elapsed time configured seconds, the PRBS Error counters will stop counting. At this time the module shall be able to present the error information collected within this gating period on Page 14h by using the Selectors 01h-05h (and 11h-15h if implemented). If 13h.Byte129.Bit4 = 0, real time error information are not updated whilst gating is in progress. The error information will only available at the end of the gate. If 13h.Byte129.Bit4 = 1, real time error information are available by using Page 14h using the Selectors 01h-05h. These real time

Required Mode of Operation	Byte 177 (D7-D0)	Description
		error information will be updated by the module every configure "y" seconds. This mode is useful if the gating period is long. A host may choose to periodically read the real-time error information during gating and take any necessary action if a bad BER is detected. To restart gating, the host has to toggle the PRBS enable registers 160 and 168 or set Page 13h.Byte177.Bit5.
Gated, nnn configured secs. Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored. If the Page 13h.Byte129.Bit2 is set, and the host writes a 1 to Bit4 of Byte 177, the gating timer will automatically restart.	xx01 *nnn*y *nnn* != 000	This behavior is the same as the above row, except for the behavior when the gate timer expires and exceeds the configured gate time. Module shall support Selectors 11h-15h to use this feature. Here at the end of the gate, that is when the individual per lane gate timer expires and exceeds the configured "nnn" elapsed time, the PRBS error information will be presented in the latched error information via the Selectors 11h-15h. The current error information will reset and the gate timer will be reset to 0 and restart accumulating errors for a new gating period. The host will have to read the error information from the previous gated time using the latched error information Selectors 11h-15h.
Restart gate timer (Bit 5)	x01x *nnn*y *nnn* != 000	This bit is used to restart all the enabled bank and lanes gate timers. When Byte177.Bit5 is set to 1b, all the enabled lanes error counters are frozen from the previous state and the gate timers are stopped. If Byte177.Bit7=0, when Byte177.Bit5 is set to 0b, all the enabled the gate timers of the current selected bank are restarted from 0 and the error information are reset and a new error accumulation gate period is restarted. If Byte177.Bit7=1, when Byte177.Bit5 is set to 0b, all the enabled the gate timers of the all banks with Byte177.Bit7=1 are restarted from 0 and the error information are reset and a new error accumulation gate period is restarted. The host may also individually toggle host Byte 160 or media Byte 168 enable bits to restart the gate timer for the host and media lanes independently. In this case, only the error information of the enable or disabled lane will reset and start count or freeze in its last value respectively.

7.6.11 Loopback Controls

Host and Media side loopback control registers and module behaviors depend on the advertised loopback capabilities in Table 7-63. Table 7-83 provides controls for loopback features in the module. The host-written loopback settings may be rejected by the module. For example, if the module advertises that it can only perform host side or media side loopback one at a time and not simultaneously, the module may reject the command and the values in the loopback controls may not change.

Table 7-83 Loopback Controls (Page 13h)

Byte	Bits	Name	Description	Type
180	7	Reserved	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Media Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all Media side lanes are in output loopback.	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media side output loopback lane 2 enable		
	0	Media side output loopback lane 1 enable		
181	7	Reserved	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Media Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all media side lanes are in input loopback.	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Media side input loopback lane 2 enable		
	0	Media side input loopback lane 1 enable		
182	7	Host side output loopback lane 8 enable	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Host Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all host side lanes are in output loopback.	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host side output loopback lane 2 enable		
	0	Host side output loopback lane 1 enable		
183	7	Reserved	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Host Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all Host side lanes are in input loopback.	RW Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	Host side input loopback lane 2 enable		
	0	Host side input loopback lane 1 enable		

7.6.12 Diagnostics Flag Masks

Table 7-84 provides masking bits for all diagnostics flags. Diagnostics flags are located on Page 14h (see Table 7-88).

Table 7-84 Diagnostics Flag Masks (Page 13h)

Byte	Bits	Name	Description	Type
206	7	M-Loss of reference clock	Loss of reference clock flag mask for the module	R/W Opt.
	6-0	Reserved		
207	7-0	Reserved		R/W
208	7	Reserved	Per-host lane gating complete flag mask. When gating is complete, this bit will be set to 1. These bits will be cleared upon pattern checker reset or disable.	R/W Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	M-Host Lane 2 Pattern Checker Gating Complete		
	0	M-Host Lane 1 Pattern Checker Gating Complete		
209	7	Reserved	Per-media lane gating complete flag mask. When gating is complete, this bit will be set to 1. These bits will be cleared upon pattern checker reset or disable.	R/W Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	M-Media Lane 2 Pattern Checker Gating Complete		
	0	M-Media Lane 1 Pattern Checker Gating Complete		
210	7	Reserved	Per-host lane pattern generator loss of lock flag mask	R/W Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	M-Host Lane 2 Pattern Generator LOL		
	0	M-Host Lane 1 Pattern Generator LOL		
211	7	Reserved	Per-media lane pattern generator loss of lock flag mask	R/W Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	M-Media Lane 2 Pattern Generator LOL		
	0	M-Media Lane 1 Pattern Generator LOL		
212	7	Reserved	Per-host lane pattern checker loss of lock flag mask	R/W Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	M-Host Lane 2 Pattern Checker LOL		
	0	M-Host Lane 1 Pattern Checker LOL		
213	7	Reserved	Latched per-media lane pattern checker loss of lock flag	R/W Opt.
	6	Reserved		

Byte	Bits	Name	Description	Type
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	M-Media Lane 2 Pattern Checker LOL		
	0	M-Media Lane 1 Pattern Checker LOL		
214-223	7-0	Reserved		R/W

7.6.13 User Pattern

Table 7-84 provides space for the host to define a user pattern of up to 32 bytes in length. The module may not support the full 32-byte length, for the maximum supported user pattern length see Table 7-70.

Table 7-85 User Pattern (Page 13h)

Byte	Bits	Name	Description	Type
224-255	7-0	User Pattern	Host defined user pattern	RW Opt.

7.7 Page 14h (Module Diagnostics 2)

Upper memory map page 14h is a banked page that contain module diagnostic advertising and control fields. The presence of Page 14h is conditional on the state of bit 5 in Page 01h byte 142 (see Table 7-39). Upper page 14h is subdivided into several areas as illustrated in Table 7-86.

Table 7-86 Page 14h Overview

Byte	Size (bytes)	Name	Description
128	1	Diagnostics Selector	This selects the content of the data in bytes 192-255
129	1	Reserved	
130-131	2	Custom	
132-139	18	Latched Diagnostics Flags	
140-149	10	Reserved	
192-255	64	Error Information Registers	Contents defined by Diagnostics Selector

7.7.1 Diagnostics Selection Register

Byte 128 on this page selects the information being displayed in bytes 192-255. The value of this byte will revert to 0 if the selected feature is not supported. Supported features are advertised in Page 13h byte 128. Valid encodings are listed in Table 7-87. For BER measurements see Table 7-89. The values in bytes 192-255 shall be updated with the selected diagnostic data within the advertised tNACK time after byte 128 has been written.

The purpose of diagnostic selection values 01-05h is for the host to be able to read the running BER whilst gating is in progress. When gating has completed, the BER of the last gated period should be reported in bytes 192-255h when a selection value of 11h-15h is chosen. The values in bytes 192-255 shall be updated with the selected diagnostic data within the advertised tNACK time after byte 128 has been written.

The purpose of diagnostic selection values 01-05h is for the host to be able to read the running BER whilst gating is in progress. When gating has completed, the BER of the last gated period should be reported in bytes 192-255h when a selection value of 11h-15h is chosen.

Table 7-87 Diagnostics Feature Encodings

Diagnostics Selection Value	Selection	Bytes 192-255 contents
00h	None	Bytes 192-255 populated with 0's
01h	Host/Media Lane 1-2 BER	Each BER is F16 format (see Section 3.3).
02h	Host Lane 1-2 error counters/Total Bits	
04h	Media Lane 1-2 error counters/Total Bits	
06h	Host and Media Lane 1-2 SNR	
07h-10h	Reserved	
11h	Latched Host/Media Lane 1-2 BER	Each BER is F16 format (see Section 3.3). (See Table 7-89)
12h	Latched Host Lane 1-2 error counters/Total Bits	
13h		
14h	Latched Media Lane 1-2 error counters/Total Bits	
16h-BFh		
C0h-FFh	Custom	

7.7.2 Latched Diagnostics Flags

The diagnostics pages include interrupt flags that are specific to diagnostics features. These interrupt flags are clear on read and behave in the same manner as non-diagnostic interrupt flags. Diagnostics interrupt flags may be masked using the mask bits in Table 7-84.

Table 7-88 Latched Diagnostics Flags (Page 14h)

Byte	Bits	Name	Description	Type
132	7	L-Loss of reference clock	Latched loss of reference clock flag for the module. Clear on Read	RO Opt.
	6-0	Reserved		
133	7-0	Reserved		RO
134	7	Reserved	Latched per-host lane gating complete flag. When gating is complete, this bit will be set to 1. These bits will be cleared on read.	RO Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	L-Host Lane 2 Pattern Checker Gating Complete		
	0	L-Host Lane 1 Pattern Checker Gating Complete		
135	7	Reserved	Latched per-media lane gating complete flag. When gating is complete, this bit will be set to 1. These bits will be cleared on read.	RO Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	L-Media Lane 2 Pattern Checker Gating Complete		
	0	L-Media Lane 1 Pattern Checker Gating Complete		
136	7	Reserved	Latched per-host lane pattern	RO

Byte	Bits	Name	Description	Type
	6	Reserved	generator loss of lock flag. Clear on Read	Opt.
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	L-Host Lane 2 Pattern Generator LOL		
	0	L-Host Lane 1 Pattern Generator LOL		
137	7	Reserved	Latched per-media lane pattern generator loss of lock flag. Clear on Read	RO Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	L-Media Lane 2 Pattern Generator LOL		
	0	L-Media Lane 1 Pattern Generator LOL		
138	7	Reserved	Latched per-host lane pattern checker loss of lock flag. Clear on Read	RO Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	L-Host Lane 2 Pattern Checker LOL		
	0	L-Host Lane 1 Pattern Checker LOL		
139	7	Reserved	Latched per-media lane pattern checker loss of lock flag. Clear on Read	RO Opt.
	6	Reserved		
	5	Reserved		
	4	Reserved		
	3	Reserved		
	2	Reserved		
	1	L-Media Lane 2 Pattern Checker LOL		
	0	L-Media Lane 1 Pattern Checker LOL		
140-149	7-0	Reserved		RO

7.7.3 Error Information Registers

The Diagnostics Selection field in Byte 128 on this page defines what values are populated in bytes 192-255 by the module. Table 7-89 provides the details of the contents of bytes 192-255 for each defined Diagnostics Selection encoding.

Table 7-89 Bytes 192-255 Contents per Diagnostics Selector (Page 14h)

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
00h	192-255	64	Reserved	
01h	192-193	2	Host side BER, lane 1	BER in F16 format (see Section 3.3) Non Zero Range is 1.000E-24 to 2.047E+10.
	194-195	2	Host side BER, lane 2	
	196-197	2	Reserved	
	198-199	2	Reserved	
	200-201	2	Reserved	
	202-203	2	Reserved	
	204-205	2	Reserved	
	206-207	2	Reserved	

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
	208-209	2	Media side BER, lane 1	
	210-211	2	Media side BER, lane 2	
	212-213	2	Reserved	
	214-215	2	Reserved	
	216-217	2	Reserved	
	218-219	2	Reserved	
	220-221	2	Reserved	
	222-211	2	Reserved	
02h	192-199	8	Host side error count lane 1	Little-endian format (LSB first) The total Bits 64 bit register, least significant bit, is to be used to indicate BER lock (real-time). Register 136 in Page 14h consist of the latched PRBS BER LOL. This reduces the read and the host can read a 64 byte block to measure BER. Example: An "Even" total bits means that the BER data calculated from error count bits / total bits can be trusted. An "Odd" total bits, means there is currently a BER lock problem. The BER rate will not be hardly affected by this because the total bits counter is usually very large.
	200-207	8	Host total bits lane 1	
	208-215	8	Host side error count lane 2	
	216-223	8	Host total bits lane 2	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	
	248-255	8	Reserved	
03h	192-199	8	Reserved	
	200-207	8	Reserved	
	208-215	8	Reserved	
	216-223	8	Reserved	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	
	248-255	8	Reserved	
04h	192-199	8	Media side error count lane 1	Little-endian format (LSB first)
	200-207	8	Media total bits lane 1	
	208-215	8	Media side error count lane 2	
	216-223	8	Media total bits lane 2	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	
	248-255	8	Reserved	
05h	192-199	8	Reserved	
	200-207	8	Reserved	
	208-215	8	Reserved	
	216-223	8	Reserved	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	
	248-255	8	Reserved	
06h	192-193	2	Reserved	
	194-195	2	Reserved	
	196-197	2	Reserved	
	198-199	2	Reserved	
	200-201	2	Reserved	
	202-203	2	Reserved	
	204-205	2	Reserved	

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
	206-207	2	Reserved	
	208-209	2	Host side SNR lane 1	Little-endian format (LSB first)
	210-211	2	Host side SNR lane 2	
	212-213	2	Reserved	
	214-215	2	Reserved	
	216-217	2	Reserved	
	218-219	2	Reserved	
	220-221	2	Reserved	
	222-223	2	Reserved	
	224-225	2	Reserved	
	226-227	2	Reserved	
	228-229	2	Reserved	
	230-231	2	Reserved	
	232-233	2	Reserved	
	234-235	2	Reserved	
	236-237	2	Reserved	
	238-239	2	Reserved	
	240-241	2	Media side SNR lane 1	Little-endian format (LSB first)
	242-243	2	Media side SNR lane 2	
	244-245	2	Reserved	
	246-247	2	Reserved	
	248-249	2	Reserved	
	250-251	2	Reserved	
	252-253	2	Reserved	
	254-255	2	Reserved	
11h	192-193	2	Latched Host side BER, lane 1	BER in F16 format (see Section 3.3) Non Zero Range is 1.000E-24 to 2.047E+10.
	194-195	2	Latched Host side BER, lane 2	
	196-197	2	Reserved	
	198-199	2	Reserved	
	200-201	2	Reserved	
	202-203	2	Reserved	
	204-205	2	Reserved	
	206-207	2	Reserved	
	208-209	2	Latched Media side BER, lane 1	
	210-211	2	Latched Media side BER, lane 2	
	212-213	2	Reserved	
	214-215	2	Reserved	
	216-217	2	Reserved	
	218-219	2	Reserved	
	220-221	2	Reserved	
	222-211	2	Reserved	
12h	192-199	8	Latched Host side error count lane 1	Little-endian format (LSB first) The total Bits 64 bit register, least significant bit, is to be used to indicate BER lock (real-time). Register 136 in Page 14h consist of the latched PRBS BER LOL. This reduces the read and the host can read a 64 byte block to measure BER. Example: An "Even" total bits means that the BER data calculated from error count
	200-207	8	Latched Host total bits lane 1	
	208-215	8	Latched Host side error count lane 2	
	216-223	8	Latched Host total bits lane 2	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
	248-255	8	Reserved	bits / total bits can be trusted. An "Odd" total bits, means there is currently a BER lock problem. The BER rate will not be hardly affected by this because the total bits counter is usually very large.
13h	192-199	8	Reserved	
	200-207	8	Reserved	
	208-215	8	Reserved	
	216-223	8	Reserved	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	
	248-255	8	Reserved	
14h	192-199	8	Latched Media side error count lane 1	Little-endian format (LSB first)
	200-207	8	Latched Media total bits lane 1	
	208-215	8	Latched Media side error count lane 2	
	216-223	8	Latched Media total bits lane 2	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	
	248-255	8	Reserved	
15h	192-199	8	Reserved	
	200-207	8	Reserved	
	208-215	8	Reserved	
	216-223	8	Reserved	
	224-231	8	Reserved	
	232-239	8	Reserved	
	240-247	8	Reserved	
	248-255	8	Reserved	

Appendix A Form Factor Specific Signal Names

Table A-1 associates SFP-DD form factor-specific terminology and signal names with generic CMIS equivalent signal names.

Table A-1 Form Factor Signal Name Associations

SFP-DD	CMIS generic name
ResetL	ResetL
NA	ModSelL
TxFault	NA
IntL/TxFaultDD	IntL
TxDisable	NA
TxDisableDD	NA
RxLOS	NA
RxLOSDD	NA
Speed1	NA
Speed2	NA
Speed1DD	NA
Speed2DD	NA
LPMode	LPMode
ePPS	ePPS

Appendix B Example Initialization Flows

This appendix includes some example flows that illustrate interactions between the host and module during module and data path initialization. Refer to section 6.3.1 for Module State Machine details and section 6.3.2 for Data Path State Machine, Application, and Control Set details.

B.1 Host Flow Examples

This section contains example flows that could be used by host implementers to power up and initialize the module and example flows that could be used by host implementers to deinitialize and power down the module.

The following example host flows are in this section.

Name	Description	Section
Quick hardware initialization	Flow showing power up and initialization with no host software interaction	B.1.1
Quick software initialization	Flow showing power up and initialization with minimal host software interaction	B.1.2
Software configuration and initialization	Flow showing power up and initialization with module configuration by host software interaction	B.1.3
Hardware deinitialization	Flow showing power-down sequence using hardware control	B.1.4
Software deinitialization	Flow showing power-down sequence using software control	B.1.5

B.1.1 Quick Hardware Initialization

The following table provides an example of a simple module power-up sequence where the module powers up under hardware control (LPMode=0) without host software intervention. This example flow has the following key attributes:

a. Module is powered-up from an un-powered state
b. Module is powered-up under hardware control (LPMode=0)
c. Host uses the default settings for the selected Application. The host does not use custom signal integrity settings (i.e. Explicit Control indicator)
d. Host does not perform speed negotiation.

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Host applies Vcc, LPMode=0, ResetL=1. Host must also ensure that host transmitters are configured to produce a stable signal that is consistent with the default Application in the module, prior to step 7 below.			
1	Hot Plug			
2	Host detects module presence, waits for IntL assertion		Module powers up and initializes management interface, setting ForceLowPwr=0, LowPwr=1 and DataPathDeinit=00h and writing the power on default data path configurations into the Active Set and Staged Set 0	M=MgmtInit D=DataPathDeactivated
3			Module sees LowPwrS transition signal is FALSE on entry into ModuleLowPwr and transitions to ModulePwrUp	M=ModuleLowPwr D=DataPathDeactivated
4			Module powers up to High Power Mode	M=ModulePwrUp D=DataPathDeactivated
5			Module sets the Module State Changed flag to 1 on entry into ModuleReady	M=ModuleReady D=DataPathDeactivated
6	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module sees DataPathDeinitS transition signal is FALSE and transitions all data path states to DataPathInit	
7	Host waits for second IntL assertion to indicate completion of data path initialization		Module initializes all data paths according to the configuration in the Active Set.	M=ModuleReady D=DataPathInit
8			Module sees DataPathDeactivateS transition signal is FALSE and transitions all data path states to DataPathTxTurnOn	M=ModuleReady D=DataPathInitialized
9			Modules enables all Tx outputs	M=ModuleReady D=DataPathTxTurnOn
10		<-	Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathActivated	M=ModuleReady D=DataPathActivated
11	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	

B.1.2 Quick Software Initialization

The following table provides an example of a simple module power-up sequence where the module powers up under software control (LPMode=1) but uses the default data path configuration. This example flow has the following key attributes:

a. Module is powered-up from an un-powered state
b. Module is powered-up under software control (LPMode=1)
c. Host uses the default settings for the selected Application. The host does not use custom signal integrity settings (i.e. Explicit Control indicator)
d. Host does not perform speed negotiation.

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Host applies Vcc, LPMode=1, ResetL=1			
1	Hot Plug			
2	Host detects module presence, waits for IntL assertion		Module powers up and initializes management interface, setting ForceLowPwr=0, LowPwr=1 and DataPathDeinit=00h and writing the power on default data path configurations into the Active Set and Staged Set 0	M=MgmtInit D=DataPathDeactivated
3		<-	Module sets the Module State Changed flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
4	Host detects assertion of IntL and reads the interrupt flag registers, which deasserts IntL		Module waits for host action	
5	Host reads module power requirements and data path configuration information			
6	Host configures and enables host transmitters such that they are producing a stable signal that is consistent with the default Application in the module			
7	Host sets LowPwr bit to 0 to initiate a module transition to High Power Mode	->		
8	Host waits for IntL assertion to indicate completion of transition to High Power Mode		Module sees LowPwrS transition signal become FALSE and transitions to ModulePwrUp	
9			Module powers up to High Power Mode	M=ModulePwrUp D=DataPathDeactivated
10			Module sets the Module State Changed flag to 1 on entry into ModuleReady	M=ModuleReady D=DataPathDeactivated
11	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module sees DataPathDeinitS transition signal is FALSE and transitions all data path states to DataPathInit	
12	Host waits for second IntL assertion to indicate completion of data path initialization		Module initializes all data paths according to the configuration in the Active Set.	M=ModuleReady D=DataPathInit
13			Module sees DataPathDeactivateS transition signal is FALSE and transitions all data path states to DataPathTxTurnOn	M=ModuleReady D=DataPathInitialized
14			Modules enables all Tx outputs	M=ModuleReady D=DataPathTxTurnOn
15		<-	Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathActivated	M=ModuleReady D=DataPathActivated
16	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	

B.1.3 Software Configuration and Initialization

The following table provides an example of a simple module power-up sequence where the module powers up under software control (LPMode=1). In this example, host software powers up the module and the data paths in two separate steps. This example flow has the following key attributes:

a. Module is powered-up from an un-powered state
b. Module is powered-up under host software control (LPMode=1)
c. Host selects one of the Applications advertised by the module
d. Host uses the default settings for the selected Application. The host does not use custom signal integrity settings (i.e. Explicit Control indicator)
e. Host uses only staged Control Set 0 to configure the module (optional Staged Control Set 1 is not used).
f. Host does not perform speed negotiation.

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Host applies Vcc, LPMode=1, ResetL=1			
1	Hot Plug			
2	Host detects module presence, waits for IntL assertion		Module powers up and initializes management interface, setting ForceLowPwr=0, LowPwr=1 and DataPathDeinit=00h and writing the power on default data path configurations into the Active Set and Staged Set 0	M=MgmtInit D=DataPathDeactivated
3		<-	Module sets the Module State Changed flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
4	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	
5	Host reads module power requirements			
6	Host writes FFh to the DataPathDeinit register to prevent automatic data path initialization when the module state reaches ModuleReady			
7	Host sets LowPwr bit to 0 to initiate a module transition to High Power Mode	->		
8	Host waits for IntL assertion to indicate completion of transition to High Power Mode		Module sees LowPwrS transition signal become FALSE and transitions to ModulePwrUp	
9			Module powers up to High Power Mode	M=ModulePwrUp D=DataPathDeactivated
10		<-	Module sets the Module State Changed flag to 1 on entry into ModuleReady	M=ModuleReady D=DataPathDeactivated
11	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	
12	Host reads Application advertising registers			

#	Host Action		Module Action	Module State (M) Data Path State (D)
13	Host writes desired ApSel code into applicable Application registers in Staged Set 0			
14	Host configures and enables host transmitters such that they are producing a stable signal that is consistent with the selected Application			
15	Host writes FFh to Apply_DataPathInit to request that the new configuration be committed to the Active Set	->		
16		<-	Module validates the configuration requested in Staged Control Set 0. If the configuration was found to be valid, the module copies the contents to the Active Control Set. If the configuration was found to be invalid the module sets the appropriate bytes in the Configuration Error Code fields.	
17	Host reads the Configuration Error Code fields to confirm that the requested configuration was verified and accepted by the module for all associated lanes of the selected Application.		Module waits for host action	
18	Host requests initialization of the newly configured data path by writing 00h to DataPathDeinit	->		
19	Host waits for IntL assertion to indicate completion of data path initialization		Module sees DataPathDeinitS transition signal is FALSE and transitions all data path states to DataPathInit	
20			Module initializes all data paths according to the configuration in the Active Set.	M=ModuleReady D=DataPathInit
21			Module sees DataPathDeactivateS transition signal is FALSE and transitions all data path states to DataPathTxTurnOn	M=ModuleReady D=DataPathInitialized
22			Modules enables all Tx outputs	M=ModuleReady D=DataPathTxTurnOn
23		<-	Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathActivated	M=ModuleReady D=DataPathActivated
24	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	

B.1.4 Hardware Deinitialization

The following table provides an example of a simple module power-down sequence where the module powers down under hardware control (LPMode transitions from 0 to 1) without software interaction. This example flow has the following key attributes:

a. Module was previously powered up under hardware control (LPMode=0)
b. At least one data path is in the DataPathActivated state

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Module is powered up with at least one data path activated. LPMode = 0, ResetL = 1		Initial conditions: Module fully configured and powered	M=ModuleReady D=DataPathActivated
1	The host releases the LPMode signal (LPMode = 1)	->	Module sees DataPathDeactivateS transition signal is TRUE and transitions all data path states to DataPathTxTurnOff	
2			Since all Tx Disable and Tx Force Squelch bits are 0, all data path states transition to DataPathInitialized without any other action	M=ModuleReady D=DataPathTxTurnOff
3			Module sees DataPathReDeinitS is TRUE and transitions all data path states to DataPathDeinit	M=ModuleReady D=DataPathInitialized
4			Module deinitializes data path resources	M=ModuleReady D=DataPathDeinit
5			Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathDeactivated	M=ModuleReady D=DataPathDeactivated
6	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module sees LowPwrExS is TRUE and transitions the module state to ModulePwrDn	
7	Host waits for second IntL assertion to indicate completion of module power down		Module reduces the module power to low power mode levels	M=ModulePwrDn D=DataPathDeactivated
8		<-	Module sets the Module State Changed interrupt flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
9	Host detects assertion of IntL and reads all interrupt flags to clear the interrupt		Module waits for host action	

B.1.5 Software Deinitialization

The following table provides an example of a simple module power-down sequence where the module powers down under software control (LPMode=1). This example flow has the following key attributes:

a. Module was previously powered up under software control (LPMode=1)
b. At least one data path is in the DataPathActivated state

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Module is powered up with at least one data path activated. LPMode = 1, ResetL = 1		Initial condition: Module fully configured and powered	M=ModuleReady D=DataPathActivated
1	The host sets the DataPathDeinit bit for all host lanes in the applicable data path to 1	->	Module sees DataPathDeactivateS transition signal is TRUE and transitions all data path states to DataPathTxTurnOff	
2			Since all Tx Disable and Tx Force Squelch bits are 0, all data path states transition to DataPathInitialized without any other action	M=ModuleReady D=DataPathTxTurnOff
3			Module sees DataPathReDeinitS is TRUE and transitions all data path states to DataPathDeinit	M=ModuleReady D=DataPathInitialized
4			Module deinitializes data path resources	M=ModuleReady D=DataPathDeinit
5		<-	Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathDeactivated	M=ModuleReady D=DataPathDeactivated
6	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	
7	Host sets the LowPwr bit to 1	->	Module sees LowPwrExS is TRUE and transitions the module state to ModulePwrDn	
8	Host waits for IntL assertion to indicate completion of module power down		Module reduces the module power to low power mode levels	M=ModulePwrDn D=DataPathDeactivated
9		<-	Module sets the Module State Changed interrupt flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
10	Host detects assertion of IntL and reads all interrupt flags to clear the interrupt		Module waits for host action	

Appendix C Examples of Diagnostic Features Usage

This Appendix contains usage recommendations for the diagnostic features on pages 13h and 14h. For use of these diagnostic features the module should be in the Module Ready state with a selected application. The data path state is not defined for these diagnostic features.

C.1 Enabling and Disabling Host (or Media) Pattern Generator

The following procedure contains the recommended set of host TWI transactions to set the module into Host side (or Media side) pattern generation mode. Host side registers are provided, with media side registers in parenthesis.

1. Write the bank and page select registers to select page 13h on the appropriate bank.
2. Set byte 177 Page 13h to desired mode of operation.
3. Write bytes 145-151 (153-159) on page 13h with the desired pattern generator configuration and lane pattern.
4. Write bytes 176-179 on page 13h with the desired control options.
5. Write byte 144, bits 1-0 (152) on page 13h to enable the pattern generator on the selected lanes.

After the above sequence of commands, the host side electrical (media side electrical or optical) output will be generating the selected pattern for the enabled lanes. NOTE: The pattern generation feature may vary by module. On some modules, when in pattern generation mode, per lane control is not provided and all lanes may be generating the pattern. On other modules, such as modules design to support break-out, the selected lanes may be in pattern generation mode while other lanes are either disabled or in normal mission mode.

6. Write byte 144, bits 1-0 (152) on page 13h to disable the pattern generator on selected host side (media side) lanes.

When pattern generation is disabled on selected lanes, those lanes are expected to revert to mission mode if possible. In some modules, mission mode can only be achieved if none of the module interfaces, host side or media side are in pattern generation mode. A module reset may be used to guarantee that the module reverts back to mission mode. Otherwise, the host has to ensure that all pattern generation modes on all lanes for both the host and media sides are disabled for these types of modules.

C.2 Enabling Host (Media) Interface Pattern Checker

The following procedure contains the recommended set of host TWI transactions to set the module into Host side (or Media side) pattern generation mode. Host side registers are provided, with media side registers in parenthesis.

1. Write the bank and page select registers to select page 13h on the appropriate bank.
2. Set byte 177 page 13h for desired mode of operation.
3. Write bytes 161-167 (169-175) on page 13h with the desired pattern checker configuration and lane pattern.
4. Write bytes 176-179 on page 13h with the desired control options.
5. Write byte 160, bits 1-0 (168) on page 13h to enable the pattern checker on the selected lanes.

When the host enables the PRBS checker, the module is expected to reset the error counters and enable the error counters to begin counting. The behavior of the error counters is defined by byte 177 on page 13h. The following section details some of the error counter configurations and their expected behavior.

To disable the pattern checker (at any time) including in the middle of a gated error count operation, the host may set byte 160, bits 1-0 (168) to 0. If the pattern checker is disabled in the middle of a gated operation, all of the error counters are undefined. Disabling in the middle of a gated count is considered an abort operation by the module.

C.2.1 Reading Pattern Checker Error Counters

There are many scenarios in which the pattern checker can be used, based on the configuration in byte 177 on page 13h. The following sections describe the recommended host write sequences for some commonly used scenarios. These recommended sequences are provided so that host and module vendors can align on usage methods to ensure compatibility across a variety of hosts and modules. Media side registers are provided in the illustrations, but these same sequences can also be applied to host side registers. The example Application for these sequences has 8 host side lanes and 4 media side lanes.

C.2.2 Not Gated (Continuous) Error Counters, Individual Lanes,

Host Selected Mode of Operation :

a. Page 13h, byte 177, bits 3-1 = 0 (not gated)
b. Page 13h, byte 177, bit 5 = 0 (do not hold checkers in reset)
c. Page 13h, byte 177, bit 7 = 0 (reset error counts per lane)
d. Page 13h, byte 129, bit 4 = 0
    - Page 13h, byte 177, bit 0 = X. (disable)

Host write sequence:

1. Write byte 160, bits 1-0 (168) on page 13h to enable the pattern checker on selected media side lanes.
    a. The module will apply the configuration and control options to the enabled lanes.
    b. Since the configuration is not gated and polling is disabled, the Latest Error counters are available "on demand" when the host reads the current pattern checker data.
2. Write 14h to the page select register. Since error information is on demand, module may take additional time to respond with the selected diagnostics data.
3. Write the Diagnostics Selector in byte 128 on page 14h to 02h (04h) to select lanes 1-2 for the host side (media side)
4. Module will perform a read of the pattern checker error counters when byte 128 is written. (Module will not clear the error counters.)
5. Read byte 138 (139) on page 14h to ensure the pattern checker has not lost lock.
6. Read bytes R192-255 to obtain error counters and total bits.

C.2.3 Not Gated (Continuous) Error Counters, Individual Lanes, Reset Error Counter

Configuration assumptions:

a. Page 13h, byte 177, bits 3-1 = 0 (not gated)
e. Page 13h, byte 177, bit 5 = 0 (do not hold checkers in reset)
f. Page 13h, byte 177, bit 7 = 0 (reset error counts per lane)
g. Page 13h, byte 129, bit 4 = 1 (polling enabled)
    - Page 13h, byte 177, bit 0 = 0. (poll every 1 sec.)

Host write sequence:

1. Write byte 160, bits 1-0 (168) on page 13h to enable the pattern checker on selected media side lanes.
    a. The module will apply the configuration and control options to the enabled lanes.
    b. Since the configuration is not gated and polling is enabled, the module may provide the error information from the last polling period.
    c. Error counters may also available "on demand" when the host reads the current pattern checker data but this behavior is purposely left to be vendor dependent.
2. Write 14h to the page select register. To provide better response to host, the module may return the last polled error information.
3. Write the Diagnostics Selector in byte 128 on page 14h to 02h (or 04h) to select lanes 1-2 for the host side (media side)
4. Read byte 138 (139) on page 14h to ensure the pattern checker has not lost lock.
5. If the host wants to reset the error information, the host shall set 13h.Byte177.Bit5 to 1. When set:
    a. Module (may also read from the data path chips and then) freezes the current error information.
    b. Module copies current internal pattern checker counters into the latched counters.
6. Host may write the Diagnostics Selector in byte 128 on page 14h to 11h-15h to select and read the

latched error information, by reading bytes 192-255 in Page 14h for the latched BER, error counters and total bits.

7. If the host wants to restart the error counter, the host shall set 13h.Byte177.Bit5 to 0. This will reset the current error information in selector 01h-05h without affecting the latched error information in 11h-15h.

C.2.4 Not Gated (Continuous) Error Counters, All Lanes, all banks

Configuration assumptions:

a. Page 13h, byte 177, bits 3-1 = 0 (not gated)
b. Page 13h, byte 177, bit 5 = 0 (do not hold checkers in reset)13h
c. Page 13h, byte 177, bit 7 = 1 (reset error counts on all banks all enabled lane)13h
d. Page 13h, byte 129, bit 4 = 0 (polling enabled)
    - Page 13h, byte 177, bit 0 = 1. (poll every 5 sec.)

Host write sequence:

1. Write byte 160, bits 1-0 (168) on page 13h to enable the pattern checker on selected media side lanes.
    a. The module will apply the configuration and control options to the enabled lanes.
    b. Since the configuration is not gated and polling is enabled, the module may provide the error information from the last polling period.
    c. Error counters may also available "on demand" when the host reads the current pattern checker data but this behavior is purposely left to be vendor dependent .
2. Write 14h to the page select register. To provide better response to host, the module may return the last polled error information.
3. Write the Diagnostics Selector in byte 128 on page 14h to 02h (04h) to select lanes 1-2 for the host side (media side).
4. Host should read byte 138 (139) on page 14h to ensure the pattern checker has not lost lock.
5. If the host wants to reset error information, , the host shall set 13h.Byte177.Bit5 to 1. When set:
    a. Module (may also read from the data path chips and then) freezes the current error information. Since this bank's byte 177, bit 7 is set, the module will also freeze the current error information of all enable banks with Byte 177 bit 7 set.
    b. Module copies current internal pattern checker counters into the latched counters. Again here the module will copy error information of all enable lanes and banks with Byte 177 bit 7 set to the latched error information.
6. Host may write the Diagnostics Selector in byte 128 on page 14h to 11h-15h to select and read the latched error information of all banks, by reading bytes 192-255 in Page 14h for the latched BER, error counters and total bits of the respective bank.
7. If the host wants to restart the error counter, the host shall set 13h.Byte177.Bit5 to 0. This will reset the current error information in selector 01h-05h without affecting the latched error information in 11h-15h.

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